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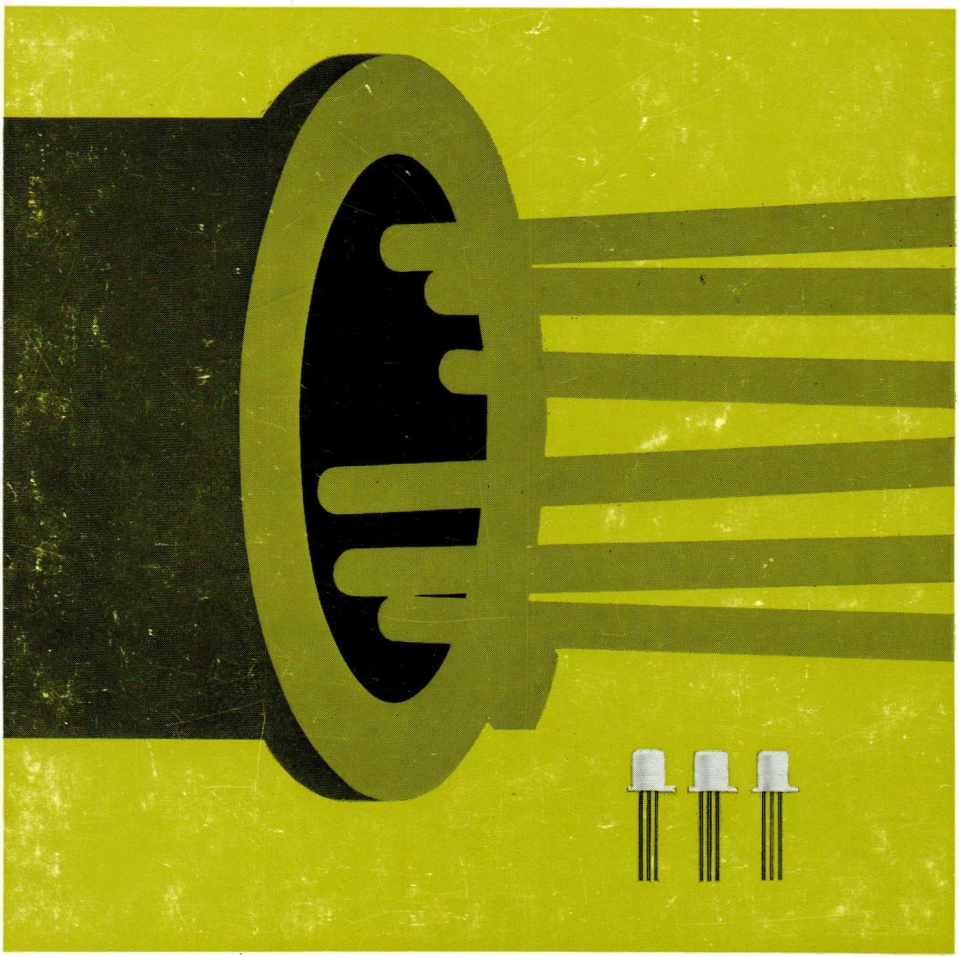
PHILIPS ELECTRONIC COMPONENTS AND MATERIALS DIVISION

CIRCUITS USING LOW-DRIFT TRANSISTOR PAIRS

BCY87 BCY88 BCY89



Circuits using Low-Drift Transistor Pairs

BCY87, BCY88, BCY89

Technical Publications Department
ELECTRONIC COMPONENTS AND MATERIALS DIVISION

The information contained herein has been
taken from the Mullard book of the same title

FOREWORD

The BCY87, BCY88 and BCY89 devices are matched pairs of n-p-n silicon planar transistors. Each pair is encapsulated in a TO-71 envelope (six-lead TO-18) which ensures good thermal coupling, and makes the transistors particularly suitable for use in directly coupled d.c. amplifiers. The transistors can also give a good performance in some switching and comparator circuits. Several circuits are described in this book, including a detailed design example of a directly coupled amplifier. The principles of d.c. amplifiers have been discussed in our publication 'Directly Coupled Amplifiers, BCY55' (ref. 1), which is available on request (order number 29-066.BE).

CONTENTS

CHAPTER 1

THE BCY87, BCY88 AND BCY89

The BCY87, BCY88 and BCY89 are matched pairs of n-p-n silicon planar transistors intended for use in differential input stages in d.c. amplifiers. Each transistor pair is encapsulated in a TO–71 envelope (six-lead TO–18), which ensures that the thermal resistance between the two transistors is very low.

The main difference between the three types is in their matched characteristics. The BCY87 is intended for input stages where low offset, drift and noise are important; the BCY88 is suitable for either input or second stages where the drift requirements are less stringent; the BCY89 is also intended for second stages and, in addition, can be used for general-purpose applications, such as switching and the comparison of two d.c. voltage levels.

MATCHED CHARACTERISTICS

The matched characteristics of the BCY87 family transistors are shown in Table 1. The characteristics apply when the collector-base voltages of the two transistors are equal, and do not exceed 10V, and also when the sum of the two emitter currents is between 10 and 100μA. Graphical representations of the characteristics are shown in Figs. 1 and 2.

TABLE 1

Matched Characteristics of the BCY87 Family

	BCY87		BCY88		BCY89		
	min	max	min	max	min	max	
$I_{C(1)}/I_{C(2)}$ $V_{BE(1)} = V_{BE(2)}$	0·90	1·11	0·80	1·25	0·67	1·50	
$\lvert V_{BE(1)} - V_{BE(2)} \rvert$ $I_{C(1)} = I_{C(2)}$	—	3·0	—	6·0	—	10	mV
$\lvert I_{B(1)} - I_{B(2)} \rvert$ $V_{BE(1)} = V_{BE(2)}$	—	25	—	80	—	300	nA

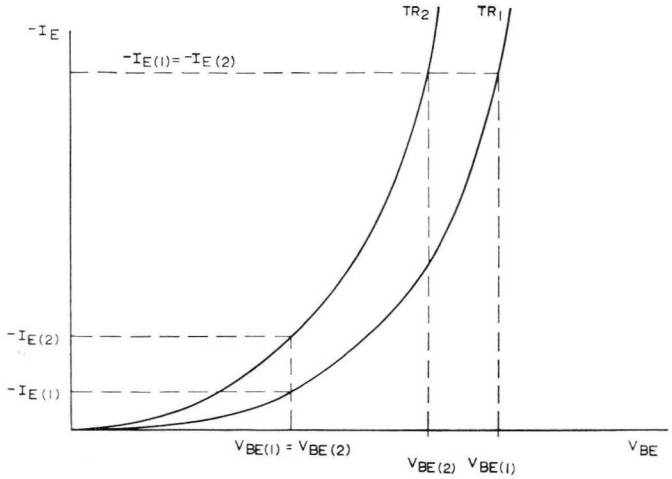


Fig. 1—Variation of emitter current with base-emitter voltage for the BCY87 family. The ratio of the emitter currents of the two transistors, and the difference between their base-emitter voltages are related by the equation

$$\frac{I_{E(2)}}{I_{E(1)}} = \exp.\left(\frac{q}{kT}|V_{BE(1)} - V_{BE(2)}|\right)$$

where $I_{E(2)}/I_{E(1)}$ is measured when

$$V_{BE(1)} = V_{BE(2)},$$

and $|V_{BE(1)} - V_{BE(2)}|$ is measured when

$$I_{E(1)} = I_{E(2)}.$$

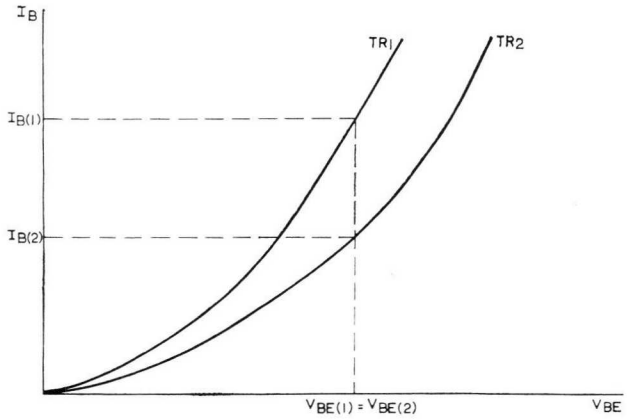


Fig. 2—Variation of base current with base-emitter voltage for the BCY87 family

Temperature Effects

The matched characteristics of the BCY87 family result in very low differential voltage and current changes with temperature. The variation in base-emitter voltage with temperature of one transistor almost equals that of the other, and the resulting differential voltage change with temperature, which is defined as

$$\frac{\delta(|V_{BE(1)} - V_{BE(2)}|)}{\delta T},$$

is shown in Table 2. The values apply over an ambient temperature range from —20 to +90°C.

Also as a result of the matched characteristics, the variation in base current of one transistor almost equals that of the other. The differential current change with temperature, defined as

$$\frac{\delta(|I_{B(1)} - I_{B(2)}|)}{\delta T},$$

is also shown in Table 2. The values again apply over an ambient temperature range from —20 to +90°C.

OPERATION OF THE BCY87 FAMILY

The BCY87 family transistors are intended for differential input stages in d.c. amplifiers, where their matched characteristics result in very low drift with temperature. To achieve the excellent performance of which the devices are capable, the transistors must be operated under the

TABLE 2

Differential Voltage and Current Changes with Temperature of the BCY87 Family

T_{amb} = —20 to +90 °C

	BCY87		BCY88		BCY89		
	typ	max	typ	max	typ	max	
$\frac{\delta(\lvert V_{BE(1)} - V_{BE(2)}\rvert)}{\delta T}$	1·0	3·0	2·0	6·0	4·0	10	μV/degC
$\frac{\delta(\lvert I_{B(1)} - I_{B(2)}\rvert)}{\delta T}$	—	0·5	—	2·0	—	10	nA/degC

correct conditions. The matched characteristics apply only when the sum of the emitter currents is between 10 and 100μA, and the collector-base voltages are between 0·5 and 10V. The circuit must therefore be designed so that both transistors operate under these conditions. The high current gain of these transistors makes operation possible at collector currents as low as 5μA, and the minimum value of h_{FE} for the individual transistors of the BCY87 is 80 at a collector current of 5μA and a collector-base voltage of 10V. The BCY87, BCY88 and BCY89 all have h_{FE} values of 100 minimum and 450 maximum at a collector current of 50μA and a collector-base voltage of 10V.

Base-emitter Voltages

The low differential base-emitter voltage change with temperature is realised only when the base-emitter voltages of the pair of transistors are equal. It is essential that the circuit design ensures this, and the easiest method of achieving it is shown in the simple circuit configuration in Fig. 3. When the input voltages are zero, the base-emitter voltages must be equal because both emitters are connected together, and both bases are referred to the same potential. When the input signals are applied, the base-emitter voltage equality is inevitably destroyed, and the input voltages should therefore be small (a few millivolts), so that the departure from the ideal matched conditions is not significant. Although this

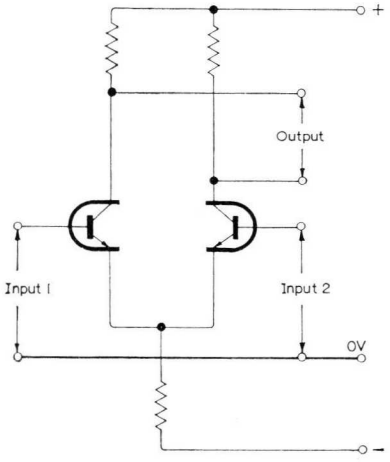


Fig. 3—Simple differential input stage using a BCY87-family transistor pair

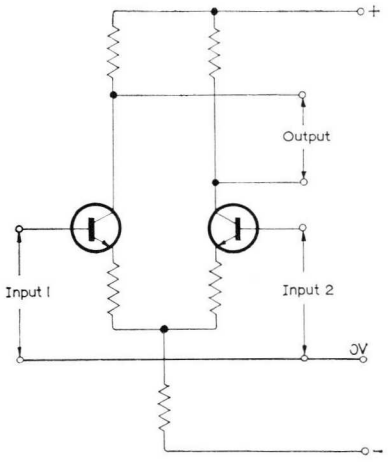


Fig. 4—Differential input stage with feedback to stabilise the gain. This circuit is not recommended—see text

appears to be a severe restriction, it should be remembered that the low drift of the BCY87 allows the amplification of small voltages. When the input voltages are larger, the performance of the BCY87 is not normally needed, and a BCY88 or BCY89 can be used.

To stabilise the gain, feedback is often applied to each half of the differential input stage as shown in Fig. 4. The introduction of a resistor in series with each emitter now makes it impossible to ensure that the transistors operate at equal base-emitter voltages. This circuit configuration should therefore not be used where low drift is required, and is not recommended for the BCY87 family.

Source Resistance

The source resistance should be low so that the drift resulting from a change in the current gain of the input transistor, and that resulting from the differential base current are kept low.

Changes in h_{FE}

From Eq. 23 on page 11 of 'Directly Coupled Amplifiers, BCY55' (Ref. 1), the equivalent change in signal voltage ∂V_S resulting from a change in the large-signal current amplification factor ∂h_{FEL} of the transistor in the first stage (its base-emitter voltage and collector cut-off current remaining constant), is given by

$$\left(\frac{\partial V_s}{\partial h_{FEL}}\right)_{V_{BE},\ I_{CBO}} = \frac{(I_C - I_{CBO})R_s}{(h_{FEL})^2},$$

where R_S is the source resistance, and I_C the collector current.

Therefore the equivalent drift at the input resulting from variations in h_{FEL} is zero when the source resistance is zero. For this reason, in practice, a very low source resistance must be used (a few hundred ohms).

Differential Base Current

The differential base current flowing through the source resistance produces an error voltage; the larger the source resistance, the larger the error voltage. The maximum differential base current change with temperature for the BCY87 is 0·5nA/degC, which produces a drift equal in magnitude to the maximum differential base-emitter voltage change with temperature (3·0μV/degC) when the source resistance is 6kΩ. Thus the source resistance should be very much less than 6kΩ (a few hundred ohms) when low drift is required.

PHYSICAL PRECAUTIONS

Because both transistors of the pair are encapsulated in the same envelope, the difference between the two junction temperatures

is very small. However, it is important to remember that the change in base-emitter voltage with temperature of a single transistor is 2mV/degC, and the differential base-emitter voltage change of the BCY87 is 1μV/degC. The figure for the BCY87 is therefore equivalent to a difference between the two junction temperatures of 0·0005degC. In other words, the junction temperatures of the two transistors must not differ by more than that amount.

In a uniform thermal environment, the close thermal coupling of the transistors ensures that the junction temperatures of the two transistors are equal. However, if a temperature gradient exists, the values for the differential voltage and current changes with temperature quoted above may not be attained. These temperature gradients can be caused by draughts of air, or they can also result from radiation. If the device is likely to be subjected to either, it should be shielded in some way.

Unwanted heat can also reach the transistors through their leads. Other components which might become warm should therefore not be mounted near the device, or anywhere where they might cause heat to be transmitted (including by radiation) to printed-wiring tracks that are connected to the device.

REFERENCE

1. **'Directly Coupled Amplifiers, BCY55'.** (Order number 29/066. August 1967)

CHAPTER 2

THE DESIGN OF A DIRECTLY COUPLED AMPLIFIER

Most directly coupled amplifiers contain at least one simple differential (or long-tailed-pair) stage, such as that shown in Fig. 5. If the changes in output current are to have no appreciable effect on the operating conditions of the long-tailed-pair, then

$$I_C \gg I_o.$$

But, for low differential voltage and current changes with temperature, I_C must be low—below 50μA for the BCY87 family.

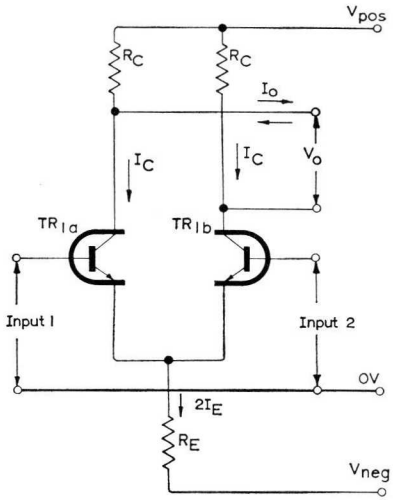


Fig. 5—Simple differential or long-tailed-pair stage

If the base-emitter voltages of the two transistors are equal, then the value of the shared emitter resistor R_E is given by

$$R_E = \frac{V_B - (V_{BE} - V_{neg})}{2I_E}$$

where V_B is the transistor base voltage (in this example zero), and $2I_E$ is approximately the sum of the two emitter currents.

For minimum drift, the collector-base voltages should be as low as possible. However, for maximum output voltage, neither transistor should bottom; that is

$$V_{CB}\text{min} = V_o\text{max} + V_{CE(\text{knee})}. \qquad \ldots(1)$$

In addition, the transistors must not bottom when a positive common-mode input is applied; that is, when a positive input signal $V_{i(c)}$ is applied to both input terminals simultaneously. Therefore

$$V_{CB}\text{min} = V_{i(c)} + V_{CE(\text{knee})}. \qquad \ldots(2)$$

Thus the minimum collector-base voltage is the larger of the two values calculated from Eqs. 1 and 2.

The value of the collector resistor R_C is given by

$$R_C = \frac{V_{pos} - V_{CB}}{I_C}.$$

The voltage gain of the stage A_v is given by

$$A_v = \frac{R_L}{r_e}$$

where

$$r_e \simeq \frac{25 \times 10^{-3}}{I_E},$$

and R_L is the parallel combination of R_C, r_i' and r_o; r_i' is the input resistance of the following stage, and r_o is the slope resistance of the collector-emitter characteristic of TR_{1a} and TR_{1b} above the knee voltage.

DESIGN EXAMPLE

The design of any amplifier starts with a specification which sets out the requirements that the amplifier has to meet. From these requirements and the knowledge of the power supply voltages, decisions can be made concerning the form of the output stage, the number of stages required and the operating conditions of the stages. Limitations set by published data or by the performance of any of the devices or components must also be taken into account. Finally, the frequency response must be shaped to meet the specification.

The following example gives the design of an amplifier excluding the shaping of the frequency response, because this depends to a critical extent on the devices used and the layout adopted.

Specification

The following specification has been chosen for an amplifier operating from +15V and −15V supplies:

Differential input	
Input resistance	$>200k\Omega$
Differential voltage drift with temperature	$<20\mu V/degC$
Single-ended output	
Output voltage for $R_L \geqslant 500\Omega$	$\pm 10V$
Output current for $R_L \leqslant 500\Omega$	$\pm 20mA$
Output resistance	$< 20\Omega$
Total voltage gain	150 000
Output voltage for zero input	0V

Outline of the Amplifier

The low output resistance required suggests that some form of emitter follower should be used for the output stage, and the shunt-compensated version is suitable. Because this cannot be driven from a long-tailed-pair, a single-ended amplifier must be interposed. This has a temperature coefficient of 2mV/degC, so the voltage gain of the stages preceding it must be at least 200 times. The single-ended stage now gives an equivalent drift at the input of one half of the required maximum of 20μV/degC.

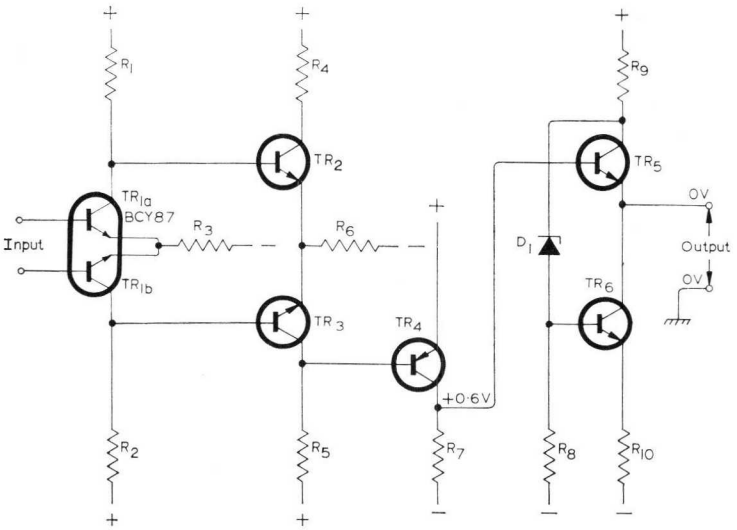


Fig. 6—Outline of amplifier used in example; the voltages shown are for zero input signal

Because a gain of 200 cannot easily be achieved in one stage, two differential amplifiers are needed.

The BCY87 is selected for use in the first stage because of its low drift performance. Because the BCY87 transistors are n-p-n, the collector voltage is positive with respect to the input (zero volts). The second stage can also be n-p-n, and then the single-ended stage must use p-n-p transistors to bring the d.c. voltage back to +0·6V. This is the voltage required by the emitter-follower output stage for an output voltage of zero volts. Thus the outline of the amplifier is as shown in Fig. 6.

Operating Conditions of the Individual Stages

The d.c. operating and signal conditions of the individual stages are so closely interrelated that, in an amplifier design, the two must be considered together. In this discussion, however, they have been separated for ease of exposition.

In the output stage, the shunt-compensated emitter follower consists of an emitter follower driving a load impedance in the normal way, together with a common-emitter amplifier in parallel with the load; the signal of the common-emitter amplifier is derived from the emitter-follower current as shown in Fig. 6. The minimum standing current through the transistors is one half the output current; in this example the minimum standing current is 10mA.

To allow for the spread in the voltage drop across the regulator diode, a nominal standing current through the transistors of 13mA is chosen, together with an emitter resistance R_{10} of 82Ω. To provide equal signal current variations in the two transistors, the collector resistance R_9 is 100Ω. With a total supply voltage of 30V, a suitable diode voltage drop is 27V. With these values, together with the need to operate the diode at a current high enough to give a low dynamic resistance, the value of R_8 is 2·2kΩ. The transistors chosen are type BC107 which have a nominal h_{FE} of 250, and therefore the d.c. input current to the stage is 50μA. The d.c. input voltage for zero output voltage is +0·6V.

Fig. 7 shows the direct currents, voltages and current gains for all the stages, and the complete circuit diagram is given in Fig. 8.

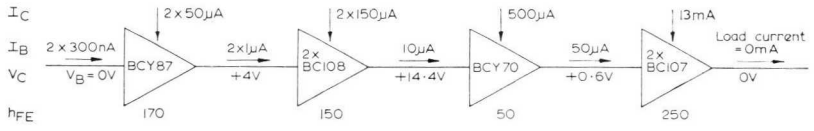


Fig. 7—Direct currents, voltages and current gains for each stage with zero input signal

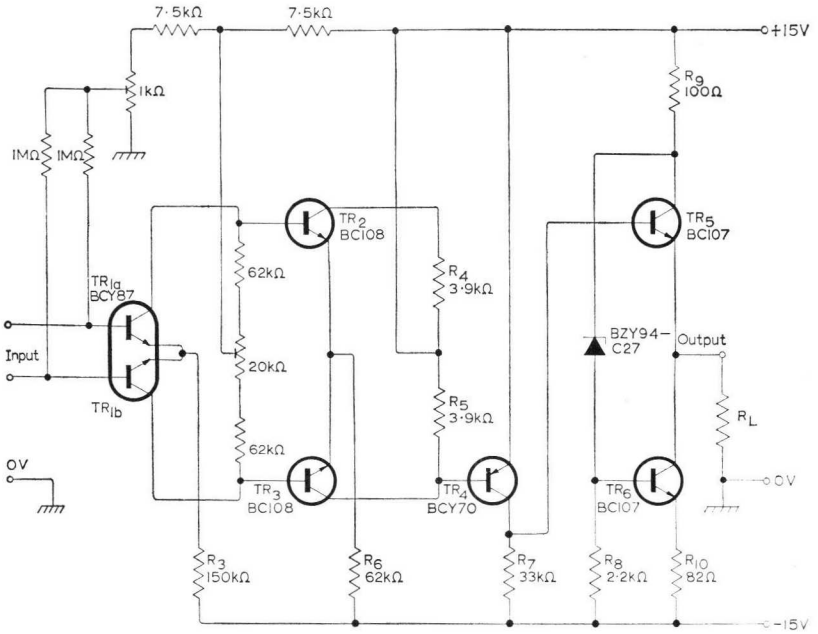


Fig. 8—Complete basic circuit of amplifier; frequency response compensation is not shown

For the single-ended stage the p-n-p transistor type BCY70 is used (TR_4). It is operated at 500μA and at this current it has a typical h_{FE} of 50; therefore a base current of 10μA is required. Because the collector supply voltage is −15V, and the d.c. potential at the input of the output stage is +0·6V, the BCY70 collector resistance R_7 becomes 33kΩ. The emitter of TR_4 is connected directly to the +15V supply, so that its base potential is

$$+15-0{\cdot}6V = +14{\cdot}4V.$$

The second stage uses two high-gain transistors type BC108 operated at collector currents of 150μA. The typical h_{FE} is 150, and thus the base currents are 1μA. The voltage across the collector resistance R_5 is the base-emitter voltage of the BCY70 (0·6V), and therefore R_5 is 3·9kΩ. To limit the collector current in the other BC108 (TR_3) during overload, it too has a collector resistor of 3·9kΩ. Because the base potentials are +4V (set by the collector potentials of the BCY87 in the first stage, as explained below) the shared emitter resistor is 62kΩ.

Each BCY87 transistor in the first stage is operated at 50μA. Because the input voltage is 0V, the base-emitter voltage of each transistor 0·5V

and the negative supply voltage —15V, the value of the shared emitter resistor is 145kΩ. The value of the collector resistors is a compromise. It should not be low compared with the input resistance of the second stage (92kΩ, see next section) otherwise the voltage gain will be low; neither should it be high, or the voltage drift caused by the current drift of the second stage will be excessive. The value chosen is 70kΩ which together with the collector potential of +4V leads to a first stage supply voltage of +7·5V. This voltage can be derived from a relatively low-resistance potential divider. The zero adjustment is incorporated in the collector circuit of this stage. It has to compensate for the difference in the collector currents of the BCY87 the difference in the base-emitter voltages of the second stage and the tolerances of the resistors. These conditions are satisfied by making the potentiometer 20kΩ and the collector resistors each 62kΩ.

Signal Conditions of the Individual Stages

The signal voltages and currents are considered for an output voltage of 1V. If the load resistance is 500Ω, the output current equals 2mA. Half of this current is contributed by the emitter follower TR_5, and therefore its signal current is 1mA. The output stage operates over a wide current range, and therefore the small-signal forward current transfer ratio (h_{fe}) is taken as 250. The input current is then 4μA at an input voltage of 1V—the voltage gain of this stage is very close to unity. The dynamic input resistance is therefore 250kΩ. These values are shown in Fig. 9 for each stage in addition to the voltage gains.

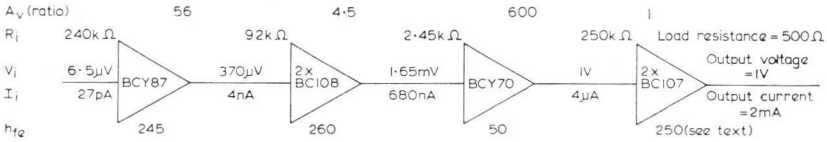


Fig. 9—Voltage gains, dynamic resistances, signal voltages, signal currents, and small-signal current gains in each stage for an output voltage of 1V

The collector resistance of the BCY70 is 33kΩ which, together with the input resistance of the output stage, gives an effective load resistance of 30kΩ. As a result the signal current is 34μA and the input current of the single-ended stage is

$$\frac{34}{50}\mu A = 680nA.$$

The voltage gain is given by

$$A_v = \frac{R_L}{\text{intrinsic emitter resistance}}$$

therefore

$$A_v = \frac{R_L}{kT/qI_E}$$

and thus, since I_C approximately equals I_E,

$$A_v = \frac{I_C R_L}{25 \times 10^{-3}}.$$

But I_C is 500μA, therefore

$$A_v = \frac{0{\cdot}5 \times 10^{-3} \times 30 \times 10^3}{25 \times 10^{-3}}$$

and

$$A_v = 600 \text{ times.}$$

The input voltage is thus 1·65mV, and the input resistance is given by

$$R_i = \frac{V_i}{I_i}.$$

Therefore

$$R_i = \frac{1{\cdot}65 \times 10^{-3}}{680 \times 10^{-9}} \Omega$$

and thus

$$R_i = 2{\cdot}45 k\Omega.$$

Calculations for the two preceding stages are made in the same way, except that the voltage gain of the second stage is effectively one half of the calculated value. This is because only half the output voltage is used in the transition from differential to single-ended operation. The values obtained from the calculations are shown in Fig. 9.

Voltage and Current Drift

The BCY87 has a typical differential voltage change with temperature of 1μV/degC, under the conditions of operation quoted above.

The second stage differential voltage drift could be as high as 30μV/degC with unselected transistors. This drift referred to the input is just over 0·5μV/degC, because the voltage gain of the first stage is 56 times. The differential current drift of the second stage probably does not exceed 1nA. This current flowing through the collector resistors of the first stage results in an equivalent voltage drift of 140μV/degC, which referred to the input becomes 2·5μV/degC.

The single-ended stage has a voltage drift of about 2mV/degC. The

combined voltage gain of the first two stages is 250 times, so that the equivalent drift input due to the third stage is

$$\frac{2\times10^3}{250}\ \text{V/degC.} = 8\mu\text{V/degC.}$$

For a rise in temperature this drift is always in the same direction while the drift due to the first two stages is random. The total drift is thus probably best expressed as $8\pm4\mu$V/degC.

Calculated Performance Compared with Requirements

It is useful to summarise the calculated performance and compare it with the specification as follows:

	Calculated value	*Requirement*
Input resistance	240kΩ	$>$ 200kΩ
Differential voltage drift with temperature	$8\pm4\mu$V/degC	$<$ 20μV/degC
Output resistance	10Ω (Measured Value)	$<$ 20Ω
Total voltage gain	150 000	150 000

The above design calculations represent what would happen under nominal conditions. A check under 'worst case' conditions can be made in exactly the same way, but substituting the appropriate values.

CHAPTER 3

CIRCUITS USING BCY87-FAMILY TRANSISTORS

GALVANOMETER AMPLIFIER

The simple galvanometer amplifier described uses a BCY87 transistor pair and two BCY72 p-n-p transistors. It amplifies a small current into one large enough to drive a robust meter.

The amplifier has been designed to give an output current of ± 1mA. It consists of a long-tailed-pair amplifier, directly coupled to two emitter followers which are connected to the output meter. A 12V power supply is used, and the current consumption is 4mA. Provision is made for adjusting the output meter current to zero for zero input voltage.

First Method of Biasing

Two methods of biasing are possible. In the one shown in Fig. 10, all the base current of one input transistor passes through the signal source.

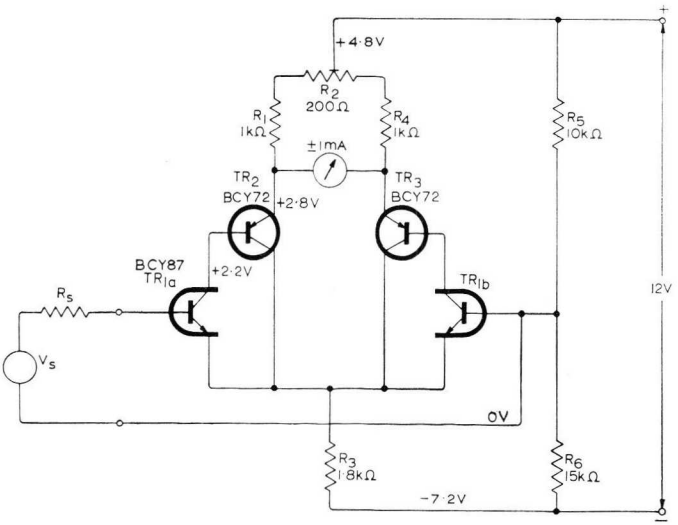


Fig. 10—Galvanometer amplifier using first method of biasing

With a 1mA meter of 10Ω resistance, the input voltage required for full-scale deflection is 30mV. With a meter of 220Ω resistance, the corresponding input voltage is 34mV.

The input current for zero output is typically 65nA, and for full-scale deflection is 90nA. Thus the dynamic input resistance r_i is given by

$$r_i = \frac{30 \times 10^{-3}}{25 \times 10^{-9}} \Omega$$

$$= 1{\cdot}2\text{M}\Omega.$$

For a 1% error in input voltage, the maximum permissible source resistance $R_s$max is 4·6kΩ. With this value of source resistance, the maximum differential base current change with temperature of the BCY87 (0·5nA/degC) causes a maximum differential voltage drift of 2·3μV/degC, which is the same order as the maximum differential base voltage change with temperature of 3·0μV/degC.

Second Method of Biasing

The circuit using the alternative method of biasing is shown in Fig. 11. Half the difference of the base currents of the input transistors passes through the signal source.

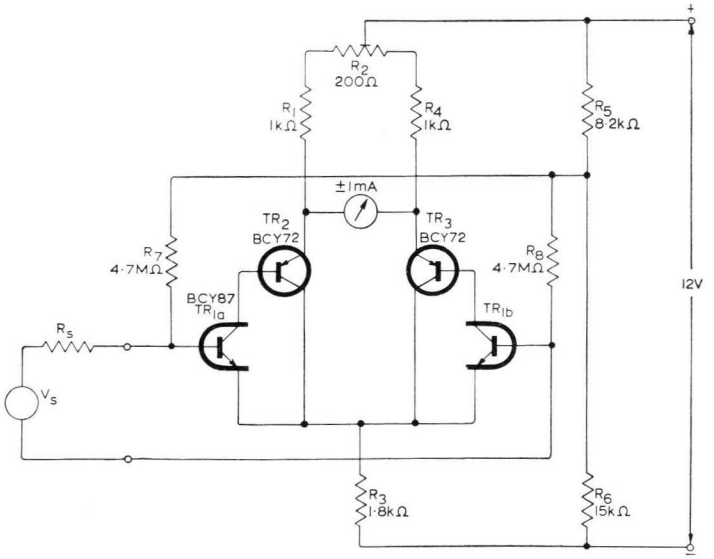


Fig. 11—Galvanometer amplifier using second method of biasing

As with the circuit in Fig. 10, the input voltage for full-scale deflection of a 1mA meter of 10Ω resistance is 30mV, and that for a meter of 220Ω resistance is 34mV.

The input current for zero output is typically between ±10nA. The change in input current for full-scale deflection is again 25nA, and thus the dynamic input resistance is again 1·2MΩ.

For a 1% error in input voltage, the maximum permissible source resistance $R_S$max is increased to 30kΩ. Because only half the base current difference flows through the source resistance, then, for a source resistance of 30kΩ, the maximum differential base current change with temperature of TR_{1a} and TR_{1b} causes a maximum differential voltage drift of

$$\frac{30\times10^{3}\times0{\cdot}5\times10^{-9}}{2}\ \text{V/degC} = 7{\cdot}5\mu\text{V/degC}.$$

This value is 2·5 times the maximum voltage drift.

AMPLIFIER WITH VOLTAGE GAIN OF 6500

Fig. 12 shows a three-stage d.c. amplifier with all stages operating in push-pull, and having an overall voltage gain of 6500 times. The input stage uses a BCY87 transistor pair. The second stage, like the first, is a long-tailed-pair amplifier (TR_2 and TR_3), but it uses two BCY71 silicon p-n-p transistors. It is directly coupled to the output stage, which is a pair of emitter followers.

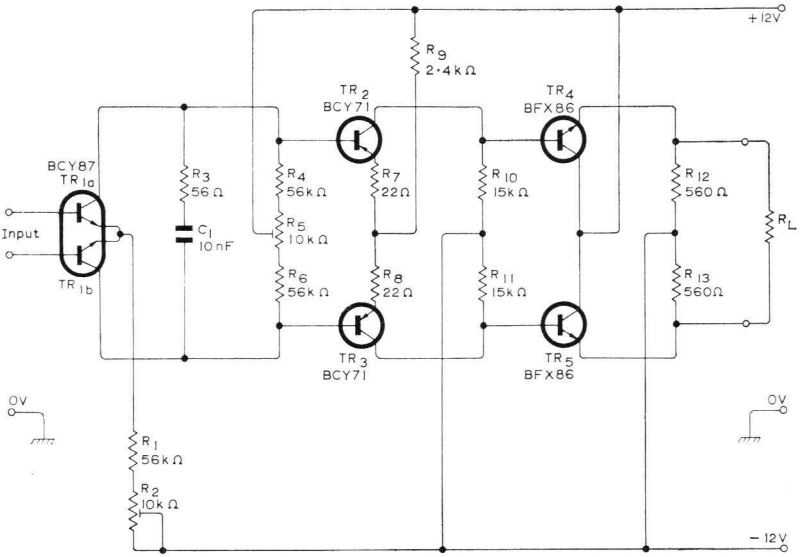


Fig. 12—Amplifier with voltage gain of 6500

The operating voltages of the first two stages have been chosen so that when there is no input signal to the amplifier, the output is also zero. This allows overall negative feedback to be applied in a simple manner without altering the d.c. conditions.

The frequency response has been shaped to fall at approximately 6dB per octave.

Measured Performance

Internal voltage gain at zero frequency	6500
	76dB
Nominal output voltage	±10V
Nominal output current	±10mA

Output voltage for zero input voltage	0V
Supply voltages	+12V, −12V
Output resistance	80Ω
Input resistance	180kΩ
Maximum common mode input voltage	5·0V
Common mode rejection ratio	45
Supply voltage rejection ratio referred to the input, for 1V change in supply voltage	200 000
Differential voltage drift with temperature, referred to the input	3μV/degC
Frequency response	see Fig. 13

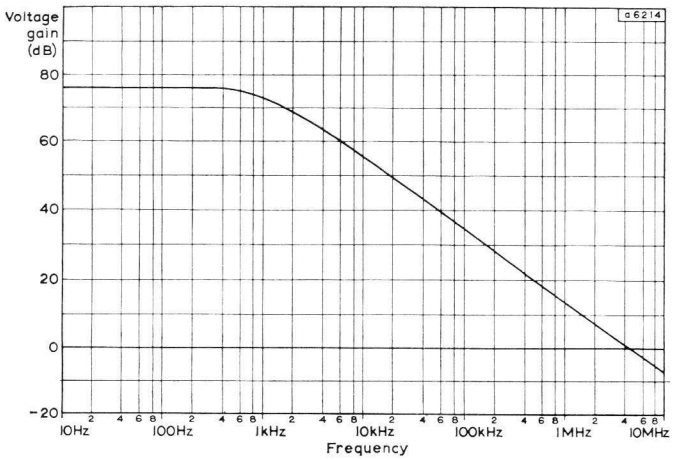


Fig. 13—Frequency response of amplifier with voltage gain of 6500

AMPLIFIER WITH VOLTAGE GAIN OF 70 000

A four-stage d.c. amplifier, with a voltage gain of 70 000 times and a single-ended output is shown in Fig. 14. The differential input stage uses a BCY87 transistor pair, with a BC107 constant-current source (TR_2) to stabilise the combined emitter currents. The outputs from this stage pass to a differential second stage which uses a BCY89 transistor pair. A single-ended output from this stage is taken to a BCY70 p-n-p transistor (TR_4), operating as a common-emitter amplifier. This drives the output stage which is a shunt-compensated emitter follower using two BC107 transistors and a BZY94–C27 voltage regulator diode.

Provision is made for setting the output voltage to zero when the input voltage is zero.

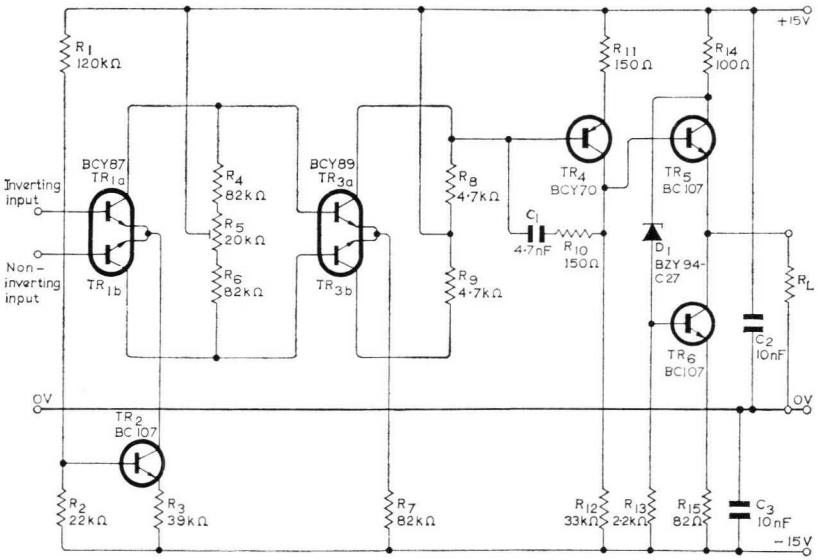


Fig. 14—Amplifier with voltage gain of 70 000

To ensure that the frequency response is the same from one amplifier to another, the two power supply lines should be decoupled to the zero-volt line within the amplifier as shown. Capacitor values of 10nF are suitable. Care should be taken to use low-inductance capacitors, and to keep their leads short.

The frequency response (Fig. 15) has been shaped to fall at approximately 6dB per octave. The amplifier is stable with parallel resistive

feedback down to an overall voltage gain of 0·1 times, and will accept a capacitive load of up to 10nF.

Measured Performance

Internal voltage gain at zero frequency	70 000 97dB
Nominal output voltage	±10V
Nominal output current	±10mA
Output voltage for zero input voltage	0V
Supply voltages	+15V, −15V
Output resistance	3Ω
Input resistance	200kΩ
Maximum common mode input voltage	10V
Common mode rejection ratio	600
Supply voltage rejection ratio referred to the input, for 1V change in supply voltage	30 000
Differential voltage drift with temperature, referred to the input	6μV/degC
Frequency response	see Fig. 15

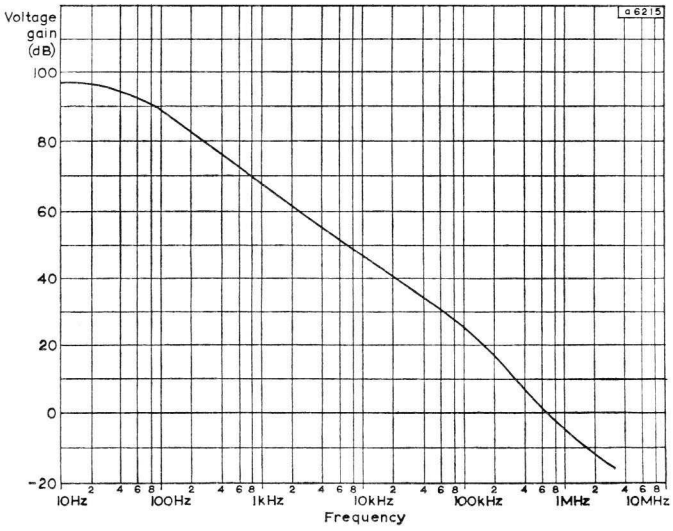


Fig. 15—Frequency response of amplifier with voltage gain of 70 000

AMPLIFIER WITH VOLTAGE GAIN OF 10^5

Fig. 16 shows a three-stage differential amplifier with a single-ended output and a voltage gain of 10^5. The first two stages are differential, the first (TR_{1a} and TR_{1b}) using a BCY87, and the second (TR_{3a} and TR_{3b}) a BCY88. The common-mode rejection ratio of the input stage is made as high as possible because it determines to a large extent the common mode rejection ratio of the amplifier. The combined emitter currents of TR_{1a} and TR_{1b} must therefore be kept constant when a common-mode input signal is applied, and to achieve this a constant-current source using a

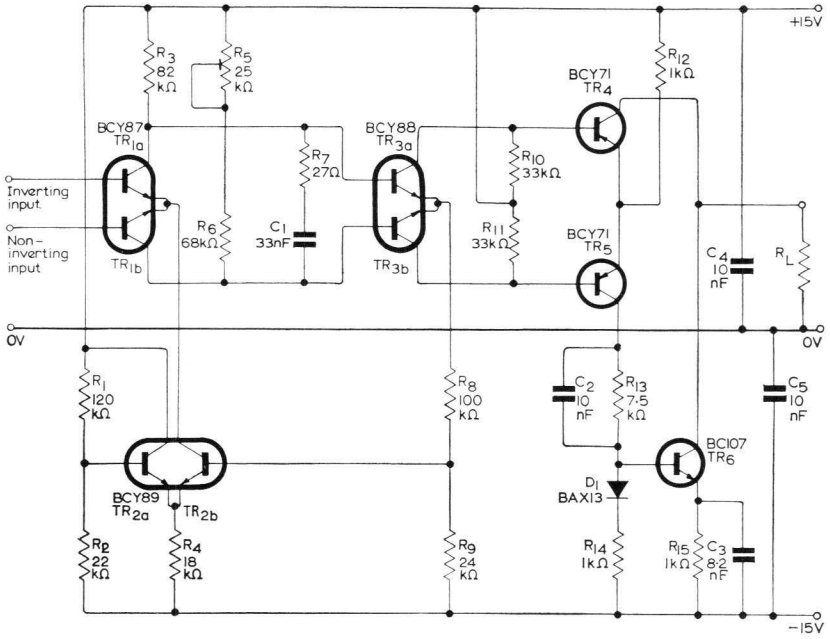


Fig. 16—Amplifier with voltage gain of 10^5

BCY89 transistor pair TR_{2a} and TR_{2b} is used. Another advantage of this circuit is that the combined emitter currents of TR_{1a} and TR_{1b} are almost independent of ambient temperature and supply voltage variations. When a common-mode input signal is applied, there will be a change in the combined emitter currents of TR_{1a} and TR_{1b}, which will cause a change in the collector potentials of TR_{1a} and TR_{1b}. This change in potential is

fed to the base of transistor TR_{2b} by means of transistors TR_{3a} and TR_{3b} and resistor R_8. Because transistors TR_{2a} and TR_{2b} are connected in a long-tailed-pair configuration, the mutual conductance of TR_{2b} is high enough to ensure sufficient negative feedback to compensate for the variation in the collector current of TR_{2b}.

The output stage uses two BCY71 p-n-p transistors TR_4 and TR_5 in a long-tailed-pair configuration. To limit the dissipation in these transistors but to provide at the same time a high load current, a variable-current source is inserted in the collector circuit of TR_4 and TR_5. The current source uses a BC107 transistor TR_6 and a BAX13 silicon diode D_1 which compensates for the base-emitter voltage of TR_6. Since the values of R_{14} and R_{15} are equal, neglecting the base current of TR_6, the currents through R_{14} and R_{15} are also equal. With no input signal, the collector currents of TR_4 and TR_5 equal the currents through R_{14} and R_{15}, and the output voltage is zero. If an input signal causes a change in the collector current of TR_4, δI_C, the collector current of TR_5 changes by $-\delta I_C$, and causes the emitter current of TR_6 to change by $-\delta I_C$. Thus the output voltage is equal to $2R_L\delta I_C$.

Preset resistor R_5 is to set the output voltage to zero for zero input.

The frequency response curve (Fig. 17) has been shaped to fall at approximately 6dB/octave. This amplifier is intended for use as an

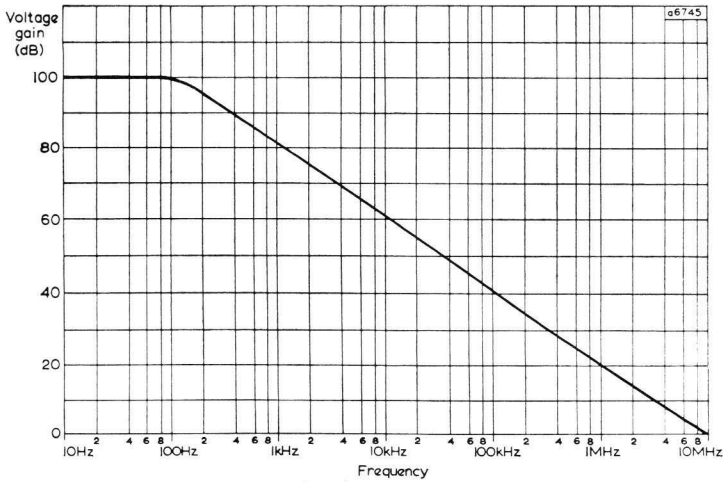


Fig. 17—Frequency response of amplifier with gain of 10^5

operational amplifier. It is unconditionally stable, and therefore free from oscillation at all values of closed-loop gain.

Measured Performance

Internal voltage gain at zero frequency	10^5
	100dB
Nominal output voltage	± 10V
Nominal output current	$\pm 2{\cdot}5$mA
Output voltage for zero input voltage	0V
Supply voltages	+15V, −15V
Output resistance	20kΩ
Input resistance	100kΩ
Maximum common-mode input voltage	± 10V
Common-mode rejection ratio	10^5
Differential voltage drift with temperature, referred to the input	3μV/degC
Frequency response	see Fig. 17

SCHMITT TRIGGER CIRCUIT

The Schmitt trigger circuit shown in Fig. 18 uses a BCY89 transistor pair. The close thermal coupling of the two transistors results in trigger (input) voltages which are more stable over a range of operating frequencies than would be obtained with transistors in separate envelopes.

Performance

The performance of the circuit was measured for sinewave drive at 10kHz, with four values of R_B ranging from 2·2kΩ to 100kΩ. The measured values of $V_{i(on)}$ and $V_{i(off)}$ are compared in Table 3 with calculated values obtained from

$$V_{i(on)} \simeq \frac{V_{pos}[h_{FE(1b)}(R_{C(1a)}+R_{C(1b)})-R_B]-R_{C(1b)}h_{FE(1b)}V_{BE(1b)}}{h_{FE(1b)}(R_{C(1a)}+R_{C(1b)})-R_B+\dfrac{R_{C(1a)}R_{C(1b)}h_{FE(1b)}}{R_E}} + V_{BE(1a)}$$

and

$$V_{i(off)} \simeq \frac{V_{pos}}{1 + \dfrac{h_{FE(1a)}R_{C(1a)}}{(1+h_{FE(1a)})R_E}} + V_{BE(1a)}.$$

The measured rise and fall times of $V_{o(1a)}$ denoted by t_r and t_f respectively are also shown in Table 3.

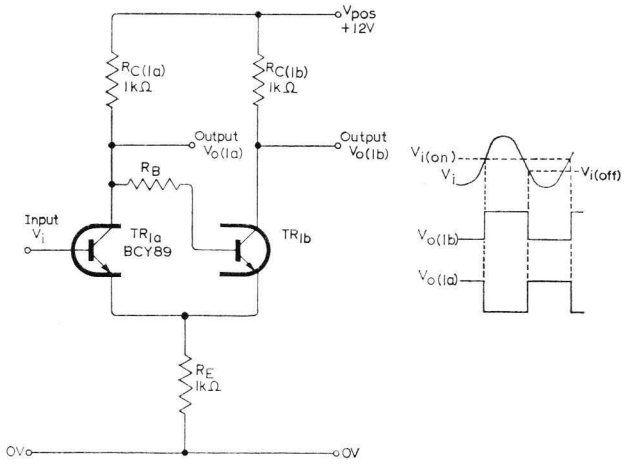


Fig. 18—Schmitt trigger

TABLE 3

Performance of Schmitt Trigger Circuit

R_B (kΩ)	Measured t_r (ms)	Measured t_f (ms)	Measured $V_{i(on)}$ (V)	Measured $V_{i(off)}$ (V)	Calculated $V_{i(on)}$ (V)	Calculated $V_{i(off)}$ (V)
2·2	0·5	0·5	8·2	6·4	8·4	6·6
10	1	1	8·1	6·5	8·4	6·6
56	3	3	7·5	6·5	8·0	6·6
100	9	7	6·4	7·0	7·6	6·6

VOLTAGE COMPARATOR

A voltage comparator circuit using BCY87 and BCY89 transistor pairs is shown in Fig. 19. The circuit operates from +12V and −12V supplies. The output voltage is limited to −0·7 and +3V, which will drive a large variety of logic circuits.

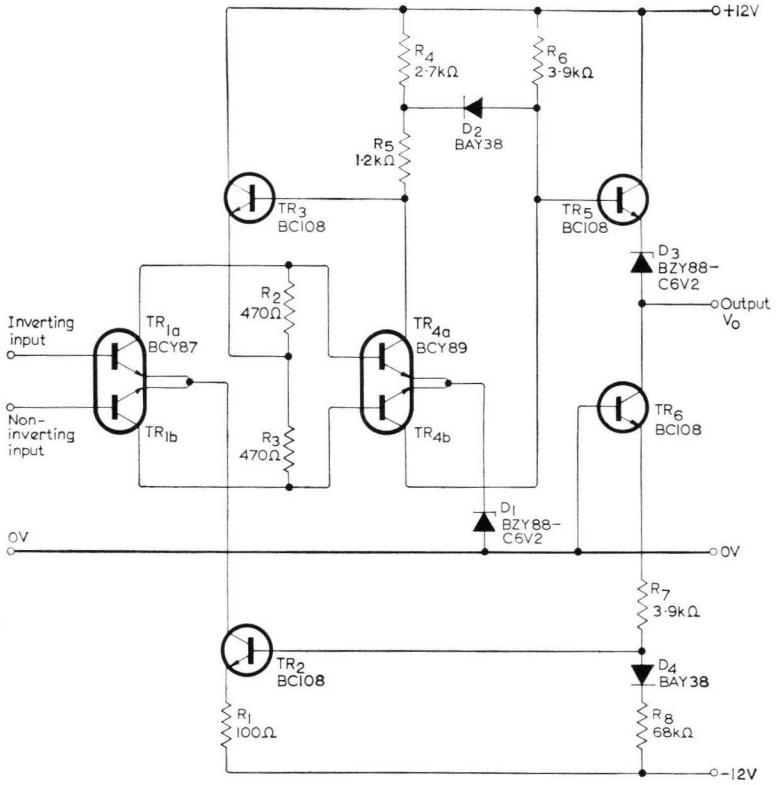


Fig. 19—Voltage comparator

Measured Performance

Transfer characteristic	see Fig. 20
Voltage gain at zero d.c. input	2000
Frequency response	see Fig. 21
Current consumption	6·8mA
Input bias current	3μA
Offset voltage	< 1mV
Differential voltage drift with temperature	1·5μV/degC

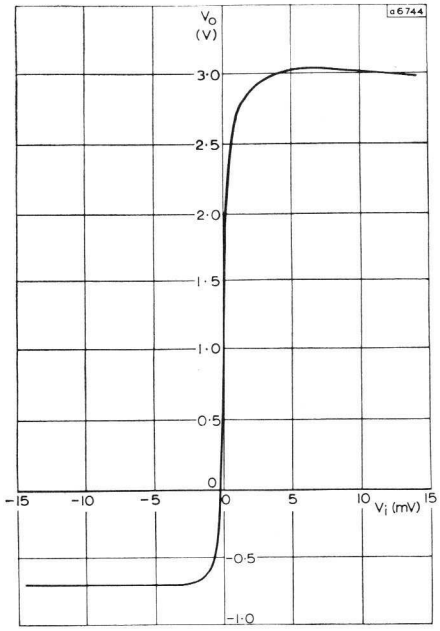


Fig. 20—Transfer characteristic of voltage comparator

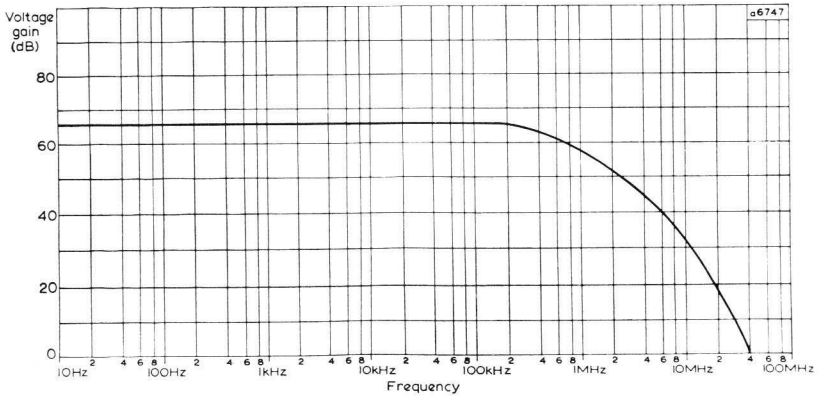


Fig. 21—Frequency response of voltage comparator

Pulse Response

The pulse response was measured using a pulse generator with rise and fall times of 1ns. The pulse was applied to the inverting input, whilst a d.c. reference signal was applied to the non-inverting input. Two sets of measurements were made with reference signals of +150mV and −150mV, and these are shown in Tables 4 and 5. The delay times, and rise and fall times were measured for values of pulse amplitude which exceeded the reference voltage by 2, 5, 10 and 20mV.

TABLE 4

Delay Times, and Rise and Fall Times for a Positive Reference and Positive-going Pulse (Negative-going Output)

Overdrive (mV)	Fall		Rise	
	Delay time (ns)	Fall time (ns)	Delay time (ns)	Rise time (ns)
2	< 5	800	50	150
5	< 5	500	120	150
10	< 5	450	200	100
20	< 5	400	350	100

TABLE 5

Delay Times, and Rise and Fall Times for a Negative Reference and Negative-going Pulse (Positive-going Output)

Overdrive (mV)	Rise		Fall	
	Delay time (ns)	Rise time (ns)	Delay time (ns)	Fall time (ns)
2	8000	1000	< 5	320
5	5500	250	< 5	330
10	3500	200	< 5	350
20	2500	200	< 5	350

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