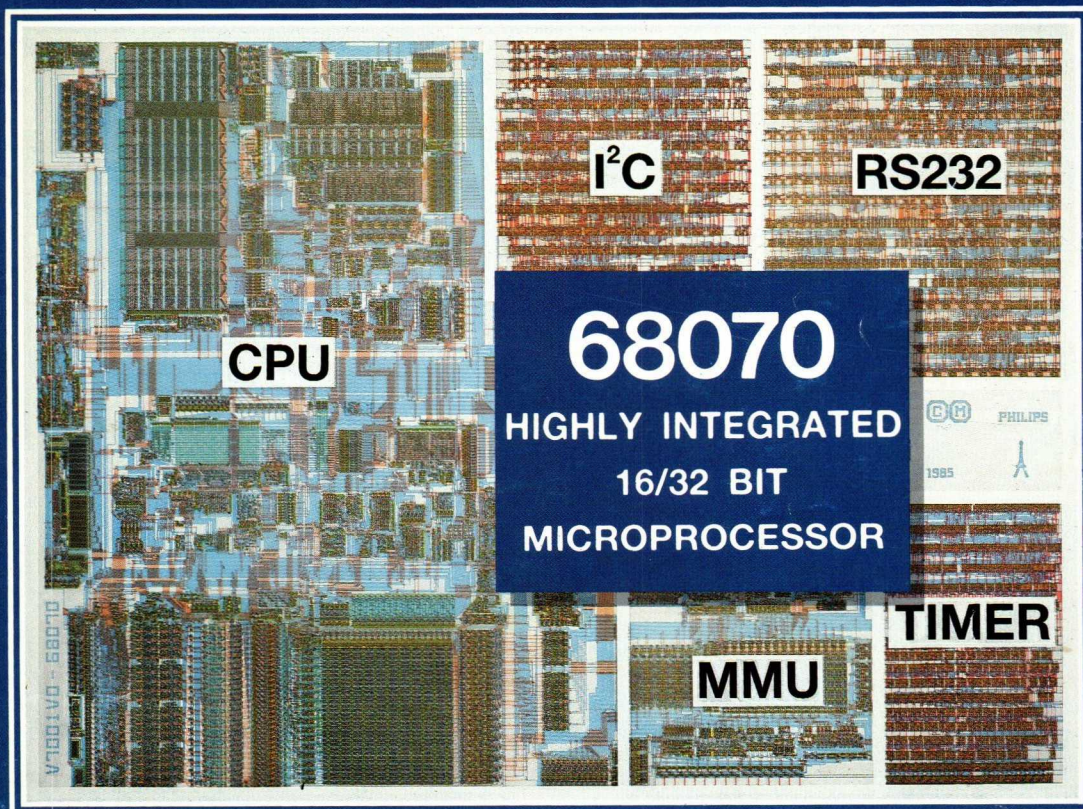


Introducing the 68070



16/32-bit microprocessor



Electronic
components
and materials

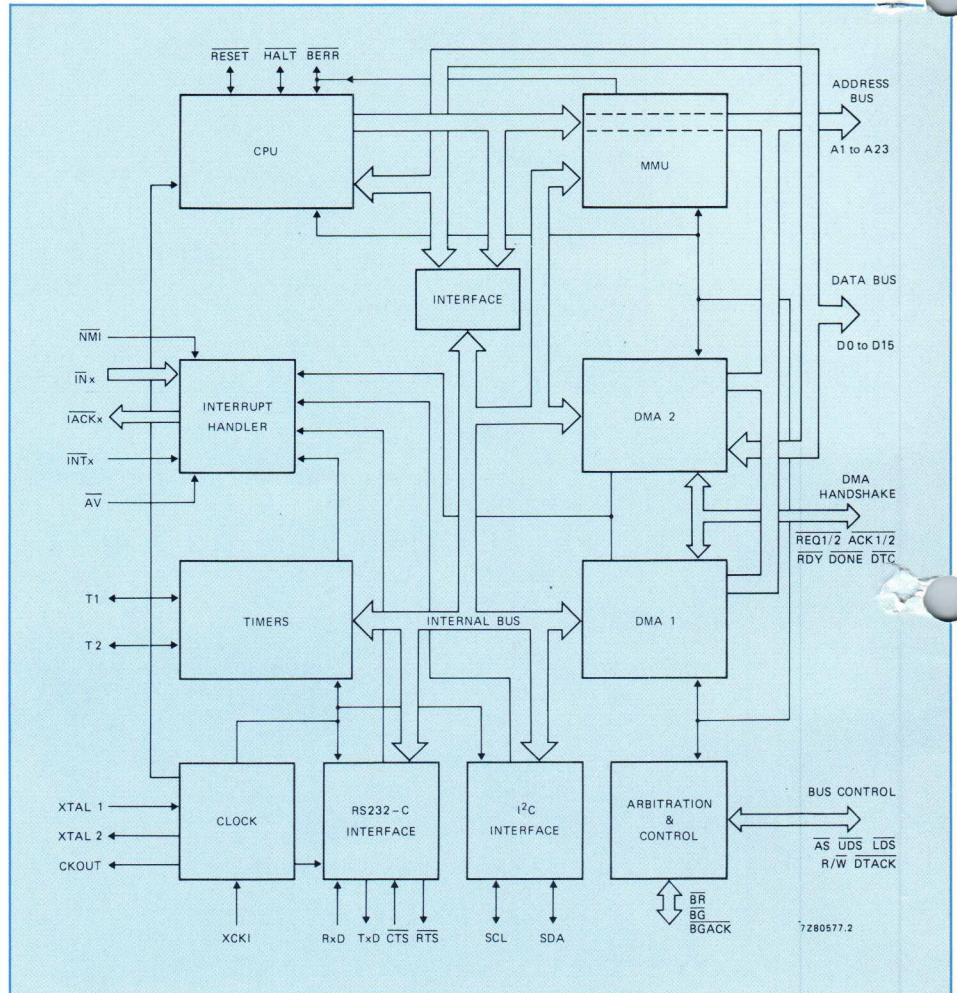
PHILIPS

FUNCTIONAL DESCR

Developed from the 68000, the generally accepted standard for mid-range work-stations, the SCC68070 is a highly-integrated microprocessor designed for the more cost-conscious market of home and personal computers, games, intelligent terminals, data communications and high-performance control.

Main Features

- CHMOS technology
- Full 68000 software compatibility
- Enhanced bus error handling
- 68000-compatible bus interface
- Same bus timing as 10 MHz 68000
- 84-pin leaded chip carrier
- 16 Mbyte addressing range
- Vectored and auto-vectored interrupts
- 4 Decoded interrupt levels
- Decoded interrupt acknowledge
- 2 programmable latched interrupts
- Built-in clock generator: 20 MHz (max) crystal
- Maximum internal clock frequency: 10 MHz
- On-chip MMU
- 2-channel DMA controller
- I²C serial bus interface
- RS232-C serial interface
- 16-bit timer
- Two 16-bit match/count/capture registers



Block diagram of the 68070

Pin Description

Power supply	V_{DD} (x2)	Supply voltage (single 5 V)	$BERR$ (I/O)	Bus error
Ground	V_{SS} (x2)		$HALT$ (I/O)	Halt
Clock	$XTAL$ 1, 2 (I) $CKOUT$ (O)	Crystal input Clock out	$RESET$ (I/O)	Reset
CPU int.cntn.	$INT1$, $INT2$ (I)	Edge-triggered interrupts	$A1...A23$ (O)	Address bus
	$IN2$, $IN4$, $IN5$ (I)	Decoded interrupt	$DO...D15$ (I/O)	Data bus
	NMI (I)	Non-maskable interrupt	$REQ1$, $REQ2$ (I)	DMA request
	$IACK2...7$ (O)	Interrupt acknowledge	$ACK1$, $ACK2$ (O)	DMA request acknowledge
	AV (I)	Auto vectored interrupts	RDY (I)	Device ready
CPU, control	AS (O)	Address strobe	DTC (O)	Device transfer complete
	LDS (O)	Lower data strobe	$DONE$ (I/O)	Done
	UDS (O)	Upper data strobe	SCL (I/O)	Serial clock
	R/W (O)	Read/write	SDA (I/O)	Serial data
	$DTACK$ (I)	Data transfer acknowledge	RxD (I)	Receive data
	BR (I)	Bus request	TxD (O)	Transmit data
	BG (O)	Bus grant	RTS (O)	Request to send
	$BGACK$ (I/O)	Bus grant acknowledge	CTS (I)	Clear to send
			$XCKI$ (I)	External clock input
			$T1$, $T2$ (I/O)	Timer output or event input

DESCRIPTION OF THE 68070

The 68070 is divided into several functional units:

- a) central processing unit (CPU)
- b) memory management unit (MMU)
- c) DMA channels
- d) serial bus (I²C)
- e) serial interface (RS232-C)
- f) capture timer

a) Central processing unit (CPU)

The 68070 CPU has a full 32-bit architecture and with the same instruction set, programming model and internal resources, the 68070 maintains full software compatibility with the 68000.

Four of its 7 interrupt levels (2, 4, 5 and 7) are provided as decoded external interrupts with separate acknowledge outputs. A further 2 latched interrupts can be programmed to a desired priority. The on-chip priority-programmable interrupts are accessed using a separate vector table.

CPU recovery from bus errors is similar to that of the 68010. When a bus error occurs, the CPU will push its internal content onto a stack prior to executing the exception routine.

b) Memory management unit (MMU)

The MMU is used to translate logical (virtual) to physical addresses and to provide segment protection against illegal access. The MMU has 8 descriptors in hardware for segment base, segment length and attributes. The MMU can handle 8 segments of up to 2 Mbytes or 128 segments of up to 128 Kbytes. Segment protection is ensured by checking the supervisor, read, write or execute permission. A stack attribute supports stack handling. When illegal access to a protected area occurs, the MMU initiates a bus error exception routine on the CPU. The MMU can be disabled by the CPU via a control register.

c) DMA channels

The 68070 has two independent DMA channels with fixed priority. The functional signals are compatible with the 68430, 68440 and 68450. The transfer (format: byte or word) is from

memory to memory (channel 2) or memory to I/O-device and vice versa (channel 1 and 2). Maximum transfer rate is 1,6 million per second in either single-cycle (cycle stealing) or burst mode, with typical latency times of less than 2,5 μ s.

d) Serial bus (I²C)

The I²C (inter-IC) bus consists of two serial lines: one carrying the clock signal and the other, the serial data. More than one device in a system may request to be bus master and after arbitration, one of the devices is recognized as such. The 68070 can operate as a receiver or transmitter in either master or slave mode. Data is transferred in bytes (excluding start and stop bits) at rates up to 100 kbits/s. The I²C interfaces directly with other I²C devices (84XX family, 84CXX family and I²C-bus IC examples on back cover).

e) Serial interface (RS232-C)

The RS232-C serial interface is a universal asynchronous data communication controller to connect to a printer, terminal or tape unit, for example. It features full duplex as well as auto echo-mode. Two baud rate

generators are programmable to one of eight transmit or receive rates (75, 150, 300, 1200, 2400, 4800, 9600 and 19600 baud), or to divide an external clock for data communication.

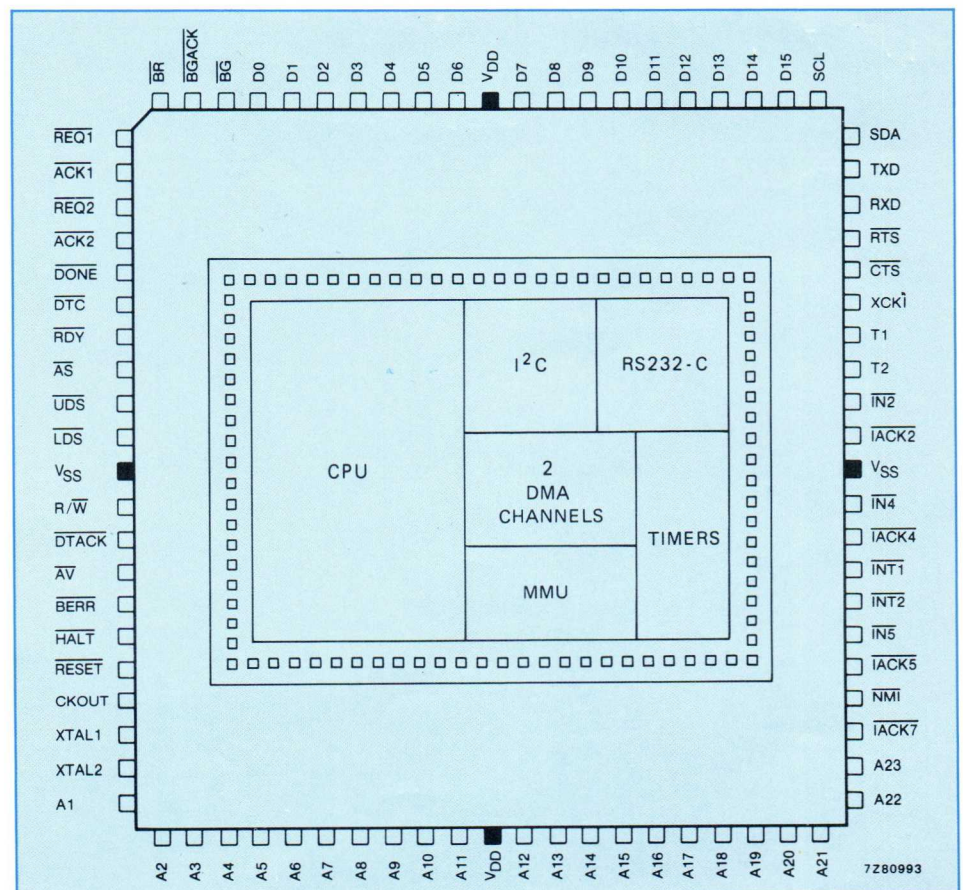
f) Capture timer

The 68070 has 3 independent 16-bit timers:

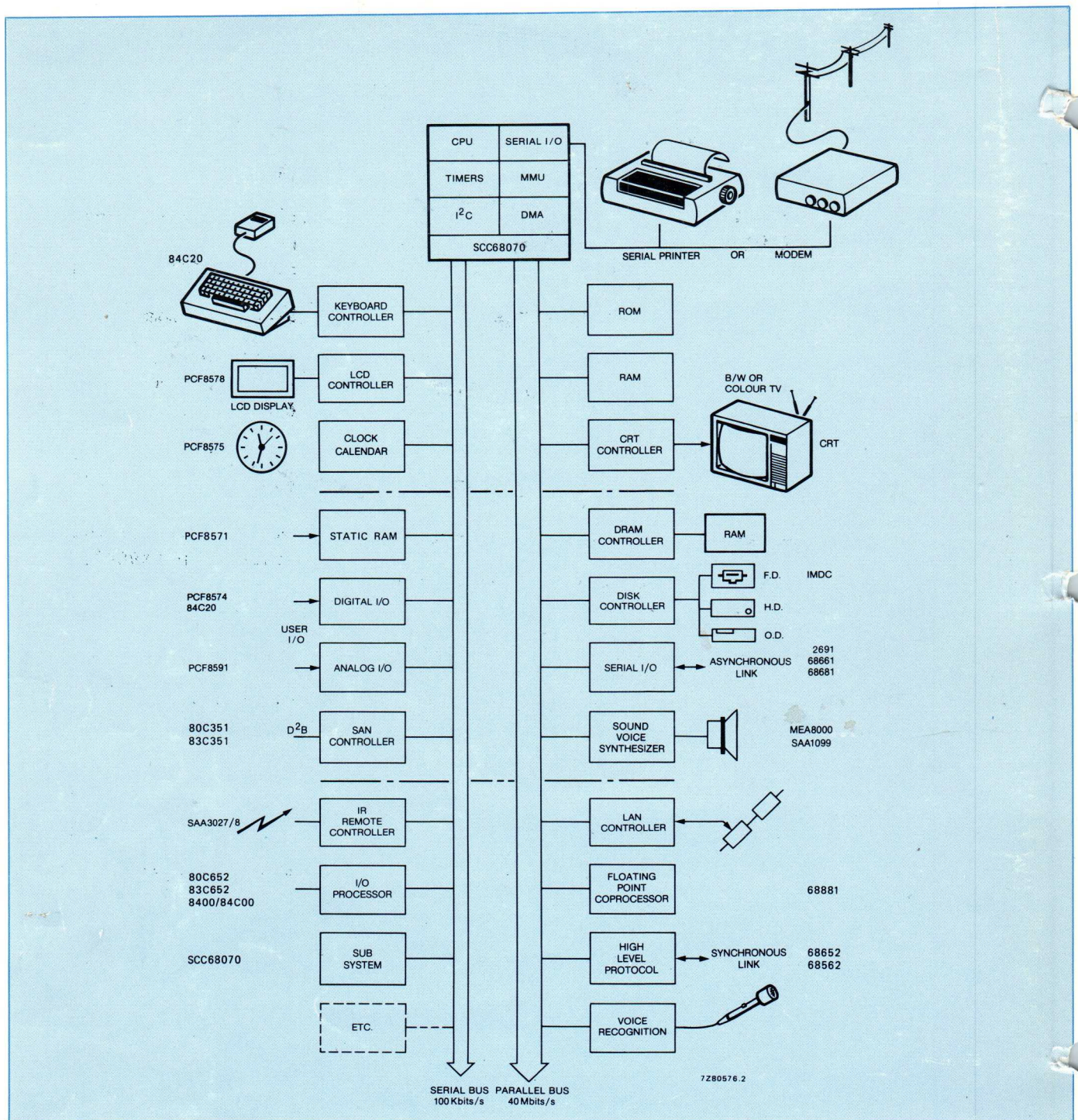
- one continuous 16-bit timer as a reference clock, 10 μ s resolution, with automatic reload on overflow
- two programmable capture timers. Each capture timer features a 16-bit register/counter that can be used in the following modes:

- 1) **Pulse generator**, to change output state when a match occurs between the reference counter and the match register.
- 2) **Event counter**, to count external events into a count register.
- 3) **Capture timer**, to store the reference timer value in the capture register when an external event occurs.

An external event can be a HIGH/LOW, LOW/HIGH or both.



Pinning diagram of the 68070



Modular extension using distributed intelligence

MORE INFORMATION FROM:

- Austria:** ÖSTERREICHISCHE PHILIPS BAUELEMENTE INDUSTRIE G.m.b.H., WIEN, Tel. 62 91 11.
- Belgium:** N.V. PHILIPS & MBL ASSOCIATED, 9 rue du Pavillon, B-1030 BRUXELLES, Tel. (02) 242 74 00.
- Denmark:** MINIWATT A/S, COPENHAGEN S, Tel. (01) 54 11 33.
- Finland:** OY PHILIPS AB, Elcoma Division, HELSINKI, Tel. 1 72 71.
- France:** R.T.C. LA RADIOTECHNIQUE-COMPELEC, PARIS, Tel. 338 80-00.
- Germany (Fed. Republic):** VALVO, UB Bauelemente der Philips G.m.b.H., HAMBURG, Tel. (040) 3296-0.
- Greece:** PHILIPS S.A. HELLENIQUE, Elcoma Division, 52, Av. Syngrou, ATHENS, Tel. 9215111.
- Ireland:** PHILIPS ELECTRICAL (IRELAND) LTD., DUBLIN, Tel. 6933 55.
- Italy:** PHILIPS S.p.A., Sezione Elcoma, MILANO, Tel. 2-6752.1.
- Netherlands:** PHILIPS NEDERLAND, Marktgroep Elconco, Postbus 90050, 5600 PB EINDHOVEN, Tel. (040) 793333.
- Norway:** NORSK A/S PHILIPS, Electronica Dept., OSLO, Tel. 68 02 00.
- Portugal:** PHILIPS PORTUGUESA S.A.R.L., LISBOA Codex, Tel. 6831 21.
- Spain:** MINIWATT S.A., BARCELONA, Tel. 3016312.
- Sweden:** PHILIPS KOMPONENTER A.B., STOCKHOLM, Tel. 08/7821000.
- Switzerland:** PHILIPS A.G., Elcoma Dept., ZÜRICH, Tel. 01-442211.
- Turkey:** TÜRK PHILIPS TICARET A.S., Elcoma Dept., P.K.504, 80074 ISTANBUL, Tel. 4359 10.
- United Kingdom:** MULLARD LTD., LONDON, Tel. 01-5806633.

This information is furnished for guidance, and with no guarantees as to its accuracy or completeness; its publication conveys no licence under any patent or other right, nor does the publisher assume liability for any consequence of its use; specifications and availability of goods mentioned in it are subject to change without notice; it is not to be reproduced in any way, in whole or in part, without the written consent of the publisher.

DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

PCB68070

16-BIT MICROPROCESSOR

GENERAL DESCRIPTION

The 68070 is a highly integrated 16/32-bit central processing unit for use in a large variety of applications and is fully software compatible with the 68000. Integrating standard as well as advanced peripheral functions on the 68070 (housed in an 84-pin package), dramatically reduces system cost.

This document gives an overview of the basic functions, internal structure, and d.c. and a.c. characteristics. For further detail on the features and operation of the 68070, refer to the "User manual PCB68070".

FEATURES

- CHMOS technology
- 32-bit internal structure
- Enhanced bus error handling
- 84-pin package
- 4 decoded interrupt inputs
- 2 programmable interrupt inputs
- Decoded interrupt acknowledge
- Built-in clock generator:
max. 20 MHz crystal
- On-chip MMU, supporting virtual memory
- 2-channel DMA controller
- I²C serial bus interface
- RS232-C serial interface
- 16-bit timer/counter
- Two 16-bit match/count/capture registers
- Full 68000 software compatibility
- 68000-compatible bus interface (10 MHz)
- 56 powerful instruction types
- 5 basic data types
- 16 Mbyte addressing range
- 14 addressing modes
- Memory mapped I/O
- Vectored and auto-vectored interrupts
- 7 interrupt levels
- Maximum internal clock frequency: 10 MHz

The internal architecture of the 68070 is built around a bus interconnecting the CPU and the various on-chip peripheral functions. Each function has several dedicated connections to the external circuitry. The 68070 includes powerful programmable interrupt processing circuitry for interrupts generated by internal and external sources. An on-chip clock generator provides a 10 MHz clock signal for CPU and peripheral interfaces.

If enabled, the on-chip MMU takes care of address translation and memory protection. Two DMA channels increase data throughput and I²C-bus interface allows easy and low-cost addition of peripherals (master and slave devices). The 68070 also includes an RS232-C interface. A built-in Timer/counter with two independently programmable MATCH/COUNT/CAPTURE registers means that the 68070 can be programmed with two of the following options simultaneously:

- pulse generator;
- external event counter;
- reference timer.

ORDERING INFORMATION

type number	temperature range	clock frequency	package
PCB68070 WP	0 to 70 °C	10 MHz	84-pin PLCC

9 091 10142



PHILIPS

November 1985

1

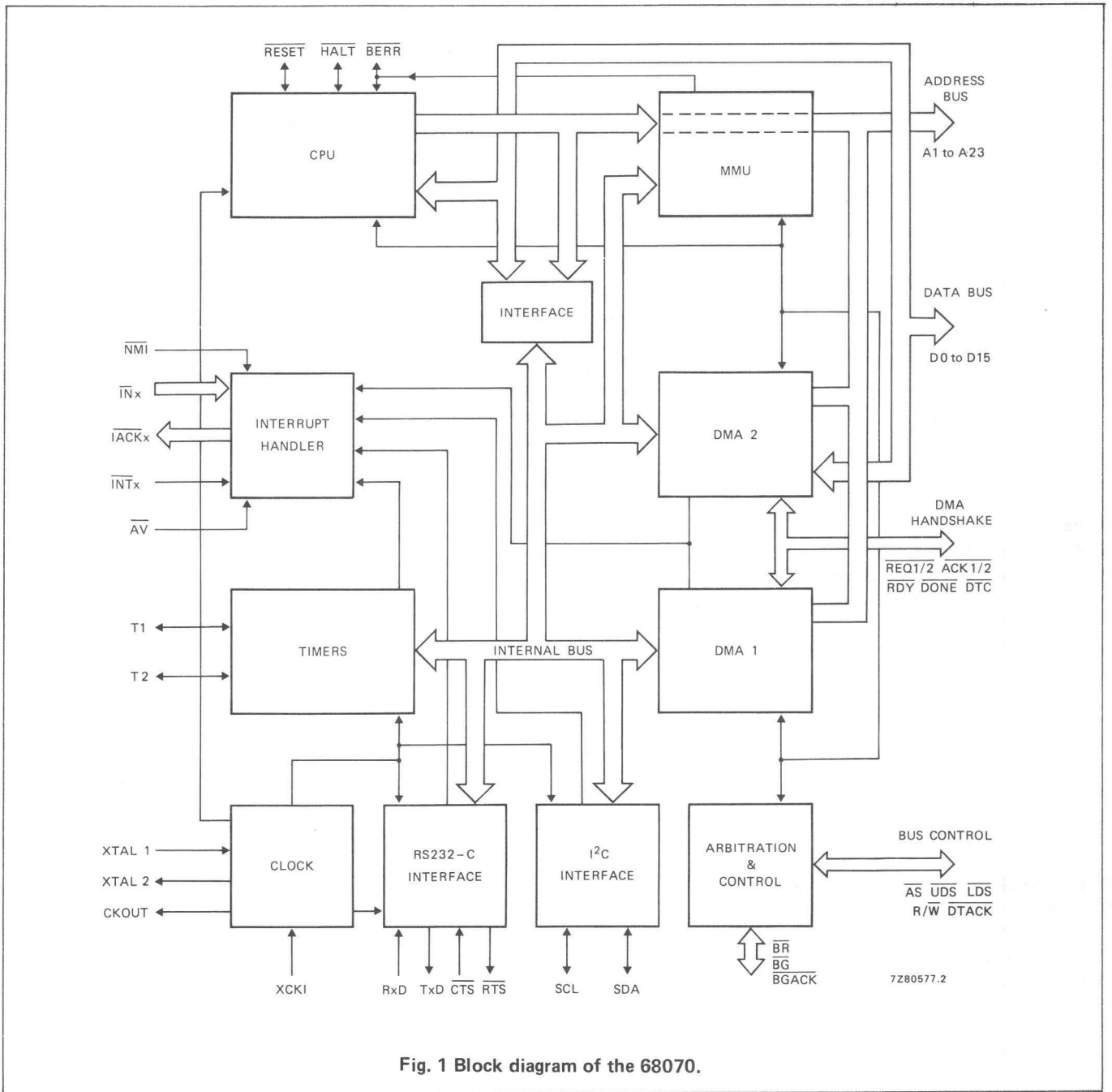
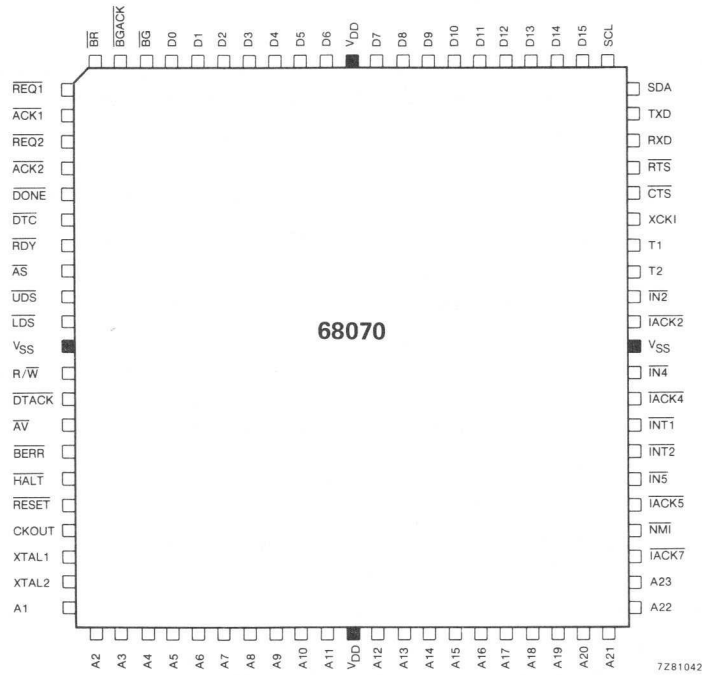


Fig. 1 Block diagram of the 68070.

SIGNAL DESCRIPTION



- NOTATION: O - Output
 I - Input
 I/O - Bidirectional
 TS - 3-state
 OD - Open-Drain
 AH - Active-HIGH
 AL - Active-LOW

Fig. 2 Pinning.

DEVELOPMENT DATA

MNEMONIC	FUNCTION
A1 to A23 O, TS, AH	Address bus for direct addressing 16 Mbytes of memory.
D0 to D15 I/O, TS, AH	16-bit wide bidirectional data bus.
\overline{AS} O, TS, AL	Address Strobe; indicates a valid address on the bus.
\overline{LDS} O, TS, AL	Lower Data Strobe; indicates that: <ul style="list-style-type: none"> - For a WRITE cycle, the data is valid on the lower half of the data bus (D0 to D7). - For a READ cycle, the data is to be placed on the lower half of the bus (D0 to D7).
\overline{UDS} O, TS, AL	Upper Data Strobe; indicates that: <ul style="list-style-type: none"> - For a WRITE cycle, the data is valid on the upper half of the data bus (D8 to D15). - For a READ cycle, the data is to be placed on the upper half of the bus (D8 to D15).
$\overline{R/W}$ O, TS	Read (active-HIGH)/Write (active-LOW); controls the direction of data flow.
\overline{DTACK} I, AL	Data Transfer Acknowledge - Asserted by the peripheral during CPU or DMA bus cycles when data is either received from or placed on the bus. If not asserted punctually, it causes the CPU or DMA controller to insert wait states.

