ORTEC
INCORPORATED
AN EG&G COMPANY

Model 715
Dual Counter/Timer

Operating and Service Manual

ORTEC

Model 715
Dual Counter/Timer

Operating and Service Manual

Printed in U.S.A.

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IMPORTANT

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STANDARD WARRANTY FOR ORTEC INSTRUMENTS

ORTEC warrants its instruments other than preamplifier FET input transistors, vacuum tubes, fuses, and batteries to be free from defects in workmanship and materials for a period of twelve months from date of shipment provided that the equipment has been used in a proper manner and not subjected to abuse. Repairs or replacement, at ORTEC option, will be made on in-warranty instruments, without charge, at the ORTEC factory. Shipping expense will be to the account of the customer except in cases of defects discovered upon initial operation. Warranties of vacuum tubes and semiconductors made by their manufacturers will be extended to our customers only to the extent of the manufacturers' liability to ORTEC. Specially selected vacuum tubes or semiconductors cannot be warranted. ORTEC reserves the right to modify the design of its products without incurring responsibility for modification of previously manufactured units. Since installation conditions are beyond our control, ORTEC does not assume any risks or liabilities associated with methods of installation or with installation results.

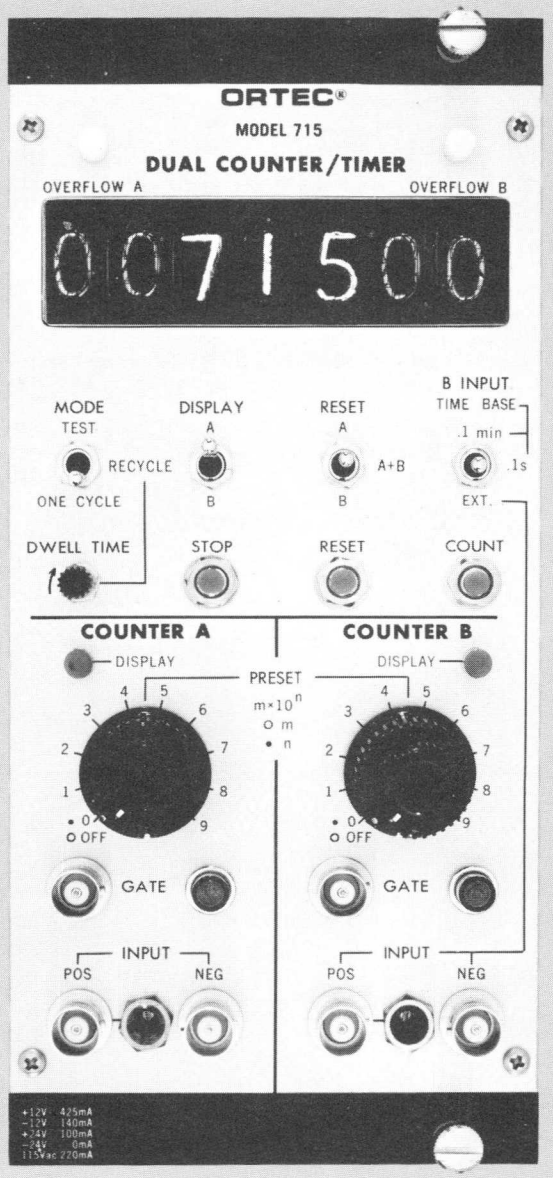
QUALITY CONTROL

Before being approved for shipment, each ORTEC instrument must pass a stringent set of quality control tests designed to expose any flaws in materials or workmanship. Permanent records of these tests are maintained for use in warranty repair and as a source of statistical information for design improvements.

ORTEC must be informed in writing of the nature of the fault of the instrument being returned and of the model and serial numbers. Failure to do so may cause unnecessary delays in getting the unit repaired. Our standard procedure requires that instruments returned for repair pass the same quality control tests that are used for new-production instruments. Instruments that are returned should be packed so that they will withstand normal transit handling and must be shipped **PREPAID** via Air Parcel Postor United Parcel. Service to the nearest ORTEC repair center. Instruments damaged in transit due to inadequate packing will be repaired at the sender's expense, and it will be the sender's responsibility to make claim with the shipper. Instruments not in warranty will be repaired at the standard charge unless they have been grossly misused or mishandled, in which case the user will be notified prior to the repair being done. A quotation will be sent with the notification.

DAMAGE IN TRANSIT

Shipments should be examined immediately upon receipt for evidence of external or concealed damage. The carrier making delivery should be notified immediately of any such damage, since the carrier is normally liable for damage in shipment. Packing materials, waybills, and other such documentation should be preserved in order to establish claims. After such notification to the carrier, please notify ORTEC of the circumstances so that we may assist in damage claims and in providing replacement equipment if necessary.


ORTEC®
MODEL 715
DUAL COUNTER/TIMER
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OVERFLOW B
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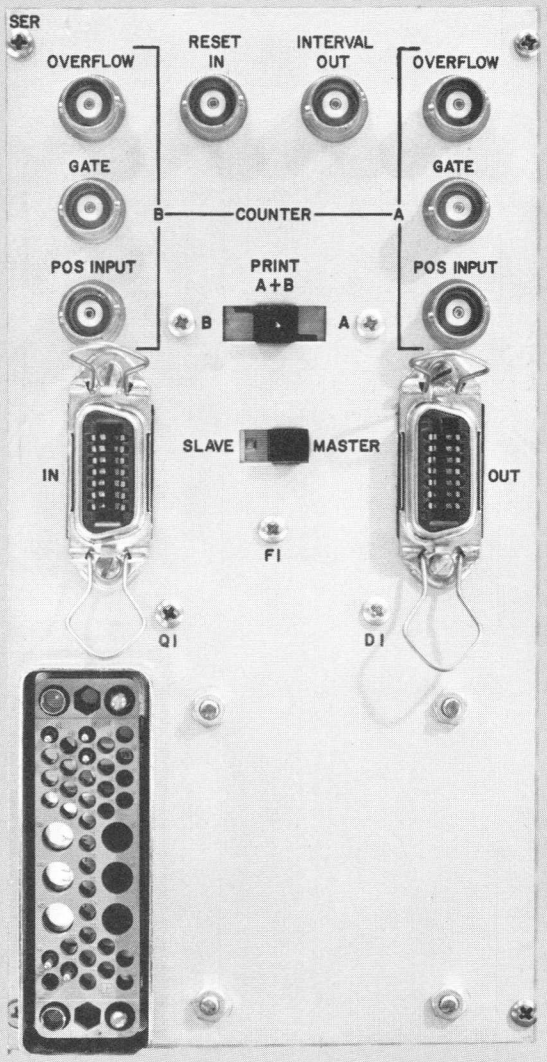
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COUNTER
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ORTEC 715 DUAL COUNTER/TIMER

1. DESCRIPTION

The ORTEC 715 Dual Counter/Timer is a flexible data accumulation module for use in general applications. It includes two counters, and a time base which can be used as the input to one of the counters when both counting and timing are desired; or both counters can count input pulses at any rate up to 20 MHz.

The ORTEC 715 may be operated as two separate counters, a counter and timer, a ratemeter, a frequency counter, a ratio counter, or a single large-capacity (13-decade) counter. It can be controlled manually or automatically, single cycled with preset stop, recycled with preset stop, self-tested, and monitored visually and/or have its accumulated data read to a printer. It is built into a standard triple-width NIM module per TID-20893 (Rev.).

Either counter can be monitored with the Nixie 7-digit display on the front panel. Counter A, at the left, is a 7-decade counter. Section B, at the right, can be used as either a counter or a timer, and has 6 decades. When it is used as a timer, it counts time increments of either 0.1 sec or 0.1 min, front-panel selectable. The time base uses the ac power line frequency.

Either one or both counters can be included in a standard ORTEC printing system or can be programmed for non-printing operation. When the 715 is used in its nonprinting mode, it can be set for One Cycle or Test or it can be set for automatic Recycle, with the dwell time front-panel adjustable between 0.3 and 10 sec. When it is used in a printing system, it can be either a Master or Slave unit, and will be recycled and read out by the program set in the 432A Printout Control.

Each counter includes a Preset count/time control with two concentric switches, a Gate input, and separate signal input connectors for positive and negative input pulses. All inputs are dc-coupled. Manual Stop and Count controls, Preset, and the equivalent printing system signals affect both counters. Reset affects either or both counters, as selected. Each counter may be gated separately.

A unique Preset circuit, separate for each counting register, permits the Preset function to be used without requiring Reset of the corresponding counting register. Thus the counting register can accumulate an integrated total of the counts in a recycling program, and the cycle can be terminated at any convenient preset level.

Each counter has a front-panel indicator and a rear-panel output to signal an Overflow. The indicator lights at the first Overflow and remains lit until its scaler is reset. There is a pulse through the rear-panel connector at each Overflow, and these pulses may be counted in the alternate section, if desired, to change the 715 into a 13-decade counter, or they may be counted in an auxiliary counter.

A rear-panel Interval Output provides a signal to indicate when either counter (or both) permits scaling.

2. SPECIFICATIONS

COUNTERS Two complete counters, identified as A and B; unless otherwise specified each item below applies equally to both counters; counter B is utilized with the time base for timing

Count Capacity Counter A - 9 999 999 = 10^7-1
Counter B - 999 999 = 10^6-1

Time Capacity 0.1-sec increments - 27.77 hr
0.1-min increments - 69.44 days

PERFORMANCE

Counting Rate 20 MHz guaranteed, 25 MHz typical

Discriminators Each positive input has an adjustable trigger level, front-panel adjustable with a potentiometer; each negative input has a fixed trigger level of -250 mV

Range +0.25 to 5 V for positive inputs

Drift <0.5 mV/°C, 0 to 50°C

Input Duty Cycle 50% max

Time Base Prescaled from power line frequency for input to Counter B in selectable increments of 0.1 sec or 0.1 min

Accuracy Same as power line frequency

Stability Same as power line frequency

Synchronizing Error <5 μsec, noncumulative, for any timing reference

Automatic Clear Generated when power is turned on initially or after power failure; used as a Reset signal, with counting mode enabled after reset

CONTROLS

MODE Three-position toggle switch selects operating mode during nonprinting operation only; when a 432A Printing Control is connected and turned on, this switch is disabled and the mode must be selected at the 432A

ONE CYCLE Upon reaching a Preset condition, the 715 will shift from a counting condition to noncounting and will remain in the noncounting condition until manually or electrically recycled.

RECYCLE Upon reaching a Preset condition, the 715 will shift from a counting condition to noncounting through the adjusted dwell time, automatically reset either or both Counters as selected by the Reset toggle, and run for a new Preset interval

TEST Selects Recycle mode and furnishes the Time Base fundamental frequency to Counter A; normal Time Base interval pulses furnished to Counter B only if Counter B is set for use as Timer

DISPLAY Toggle switch selects either Counter A or Counter B for the Nixie count level display; not effective during printout

RESET (Toggle) Three-position toggle switch permits any Reset signal to affect Counter A only, Counter B only, or both A and B

B INPUT Three-position toggle switch selects the source of signals to be counted in Counter B; selects internal Time Base intervals of 0.1 min or 0.1 sec, or External input signals

DWELL TIME Controls the display time from Preset to Reset and the return to counting during nonprinting Recycle mode operation only

STOP Manual push button stops the counting condition until it is manually started by pressing the Count switch

RESET (Push Button) Manual push button to reset either Counter, or both, as selected by the Reset toggle switch; effective only when 715 is in a noncounting condition

COUNT Manual push button to restore or initiate the counting condition

PRESET A Dual concentric selector switch selects the count level for a Preset signal in Scaler A; Preset level is $m \times 10^n$, where m is the digit selected by the outer control (1 through 9), and n is the power of 10 selected by the inner control (0 through 6); outer control set at zero ($m = 0$) is Preset Off for Counter A

PRESET B Dual concentric selector switch, same as Preset A except that the inner control includes only positions 0 through 5

DISC. A Single-turn screwdriver potentiometer sets effective discriminator level for Pos Input A signals; range +0.25 V to +5 V

DISC. B Single-turn screwdriver potentiometer sets effective discriminator level for Pos Input B signals; range +0.25 V to + 5 V

PRINT Three-position slide switch; selects Counter A only, Counter B only, or both A and B for printout

MASTER/SLAVE Two-position slide switch selects control in a scaling system

MASTER The 715 controls the mode of all Slave units in the scaling system by furnishing signals through the system gate, reset, and preset lines

SLAVE The 715 is controlled by signals through the system gate, reset, and preset lines, as well as by its individual manual and electronic gate signals

INPUTS

POS INPUT Accepts positive unipolar or bipolar signals

Amplitude From discriminator setting (+0.25- to 5-V range) to ±25 V max; ±15 V average max; can be NIM Slow Logic signals

Width 10 nsec min; no max limit

Pulse Pair Resolution 50 nsec

Rise Time No min or max limit

Input Impedance 1KΩ to ground, dc-coupled

NEG INPUT Accepts negative unipolar or bipolar signals

Amplitude -250 mV min; protected to ±100 V at 10% duty cycle; can be NIM Fast Logic signals

Width 5 nsec min; no max limit

Pulse Pair Resolution 50 nsec

Rise Time No min or max limits

Input Impedance 50Ω to ground, dc-coupled

GATE Accepts Gate logic signal to control the counter gate; neon indicator lights when counter can count

Amplitude ≥+3 V or open circuit to allow counting; ≤+1.5 V to inhibit counting; ±25 V absolute max; driving source must be capable of sinking 1.0 mA of positive current

Width 100 nsec min above +3 V; no max limit

Duty Cycle No limits

Rise Time No limits

Fall Time No limits

Input Impedance 1KΩ, dc-coupled

RESET Accepts external signal to reset either counter, or both, as selected on front panel

Amplitude NIM Standard Slow Positive Logic; ≥+3 V min to reset, ≤+1.5 V max does not reset; ±25 V absolute max

Width 500 nsec min; no max limit

Rise Time No limits

Duty Cycle No limits

Input Impedance 1KΩ, dc-coupled

OUTPUTS

OVERFLOW Provides an output pulse each time the corresponding counter overflows; a front-panel neon indicator glows continuously from the first overflow until reset

Amplitude +5 V nominal

Width ~2 μsec

Output Impedance <10 Ω, dc-coupled

INTERVAL Output signal of +3 V when either counter (or both) is in a counting interval exclusive of its Gate condition

Amplitude ≥+3 V into 100Ω indicates counting permitted; ≤+1.5 V indicates counting inhibited

Width Determined by accumulation interval width

Output Impedance <10 Ω, dc-coupled

INDICATORS

OVERFLOW A Lamp glows from first overflow of Counter A until Reset of Counter A

OVERFLOW B Lamp glows from first overflow of Counter B until Reset of Counter B

DISPLAY A Lamp glows when the contents of Counter A are shown on Nixie Display

DISPLAY B Lamp glows when the contents of Counter B are shown on Nixie Display

Nixie Display Seven-digit direct reading display monitors count level in either counter and/or each digit when it is furnished for printout

GATE A Lamp glows when Counter A is enabled to count and Gated on

GATE B Lamp glows when Counter B is enabled to count and Gated on

CONNECTORS

PRINTER IN AND OUT

Amphenol type 57-40140, rear panel only

PRINT COMMAND INPUT 1 level (for printout), +1.5 V or less, -5 V maximum; 0 level (not printing), +3 V or greater, +12 V maximum; Maximum risetime 0 to 1,10 μs

PREVIOUS MODULE FINISHED INPUT 1 level (start data transfer), +3 V or greater, +12 V maximum; 0 level, +1.5 V or less, -5 V maximum; Maximum risetime 0 to 1,10 μs

DATA OUTPUTS (1-2-4-8) 1 level, +6 V nominal (5-7) through interfacing gates; 0 level, +1 V or less clamped to ground through interfacing gate

THIS MODULE FINISHED OUTPUT 1 level, +4 V nominal (3-5); 0 level, +1 V or less

SYSTEM GATE (in & out common) 1 level (to allow counting) nominal +6 V level; 0 level (to prevent counting) +1 V or less

Note: This line can be grounded from any scaler; any external connection should be limited to an NPN transistor collector for safe operation

SYSTEM PRESET (in and out) 0 level (to allow counting) nominally +6 V; 1 level (to prevent counting) +1 V or less

Note: This line can be grounded from any scaler; any external connection should be limited to an NPN transistor collector for safe operation

SYSTEM RESET (in and out) 1 level (to cause reset) +1 V or less; 0 level (non-reset) nominally +6 V

Note: This line can be grounded from any scaler; any external connection should be limited to an NPN transistor collector for safe operation

PRINT ADVANCE (in and out) Negative pulse input from +3 V or greater to +1.5 V or less with advance occurring when signal returns positive; maximum risetime of positive transition not to exceed 10 μs

432 OFF (in and out) 1 level (MODE switch of 715 enabled), +2 V or greater, +6 V maximum; 0 level, +0.7 V or less

THIS MODULE PRINTING (in and out) 1 level (from leading edge of PREVIOUS MODULE FINISHED to end of printing of either one or both counters), +1 V or less; 0 level +6 V nominal (5-7)

POS INPUT A Type BNC (UG-1094/U), front and rear panels

NEG INPUT A Type BNC (UG-1094/U), front panel only

POS INPUT B Type BNC (UG-1094/U), front and rear panels

NEG INPUT B Type BNC (UG-1094/U),front panel only

COUNTER A OVERFLOW Type BNC (UG-1094/U), rear panel only

COUNTER B OVERFLOW Type BNC (UG-1094/U), rear panel only

GATE A Type BNC (UG-1094/U), front and rear panels

GATE B Type BNC (UG-1094/U), front and rear panels

RESET Type BNC (UG-1094/U), rear panel

INTERVAL Type BNC (UG-1094/U), rear panel

POWER Standard NIM power connector

ELECTRICAL AND MECHANICAL

Power Requirements +12 V, 430 mA; -12 V, 140 mA; +24 V, 100 mA; 115 V ac, 220 mA

Dimensions Standard triple-width module (4.05 by 8.714 in.) per TID-20893 (Rev.)

ACCESSORY INCLUDED One printing system control cable for connection with other ORTEC printing scalers, timers, digital ratemeters, etc., in a system with an ORTEC 432A Printout Control

RELATED EQUIPMENT The versatile input capability of each of the two counters in the 715 permits acceptance of either logic or linear signals from essentially any source, with either polarity. Control and connection to an external data acquisition system is obtained automatically through the rear-panel Printing Loop connectors, through an ORTEC 432A Printout Control, to an ORTEC 222 modified Teletype Page Printer.

OPTION 715-1

CRYSTAL CONTROLLED TIME BASE A separate crystal controlled time base is available as a plug-in option.

Time Base Accuracy Better than 0.0005% plus synchronizing error

Time Base Stability Better than 0.0001%/°C long term

Time Base Synchronizing Error <5 μsec, noncumulative

3. INSTALLATION

3.1 General

The 715 Dual Counter/Timer is designed for installation and operation in an ORTEC 401A/402A Bin and Power Supply, or equal. The Bin and Power Supply is designed for relay rack mounting and is usually installed in a rack that houses other electronic equipment. Therefore any vacuum tube equipment or other heat source that operates in the same rack with the 715 must be sufficiently cooled with circulating air to prevent localized heating of the transistorized and integrated circuits in the 715. The temperature of equipment mounted in racks can easily exceed 120°F (50°C), the maximum limit for safe operation of the 715, unless precautions are taken.

3.2 Connection to Power

The 715 contains an internal power supply that requires a 115-V ac input and ±12 V dc, all of which must be obtained from a Nuclear Standard Bin and Power Supply such as the ORTEC 401A/402A. Always turn off the power before inserting or removing instrument modules. The ORTEC NIM modules are designed so that a full complement of modules in the bin will not overload the bin power supply. However, this may not be true when the bin contains modules of other than ORTEC design, and power supply voltages should be checked after other modules are inserted. The ORTEC 401A/402A has test points on the power supply control panel to monitor the dc voltages.

NOTE: When using a Bin and Power Supply that is powered with 220 V ac , the ac input power required by the 715 is slightly more than the proportional share of total ac power available. Do not operate more than three 715 modules in any one such Bin and Power Supply

When using the 715 outside the 401A/402A Bin and Power Supply, be sure your extension cable includes the power supply grounding circuits specified in the recommended AEC standards of TID-20893 (Rev.). Both high-quality and power-return ground connections are specified to ensure proper reference voltage feedback into the power supply, and must be preserved in extension cable installations. Be careful to avoid ground loops when the module is not physically installed in the bin.

Some bins and power supplies, as well as extension cables, may not be wired to provide the 115-V ac power required for operation of the 715 indicators and for its integrated circuits. If the indicators fail to operate in a new installation, check the bin and/or cable to determine whether it is wired properly.

3.3 Scaler Interconnection

When a counting system contains more than one 715 Dual Counter/Timer and/or another ORTEC printing system instrument, connect the units together in a loop as shown in Figure 3-1. The connectors for this hookup are located on the rear panel of each instrument. For nonprinting systems the sequence of connection is not important, but for printing systems the order of printing is from 1 through *n* in sequence as shown in Figure 3-1. The system can include any number of modules in the loop up to a maximum of 50.

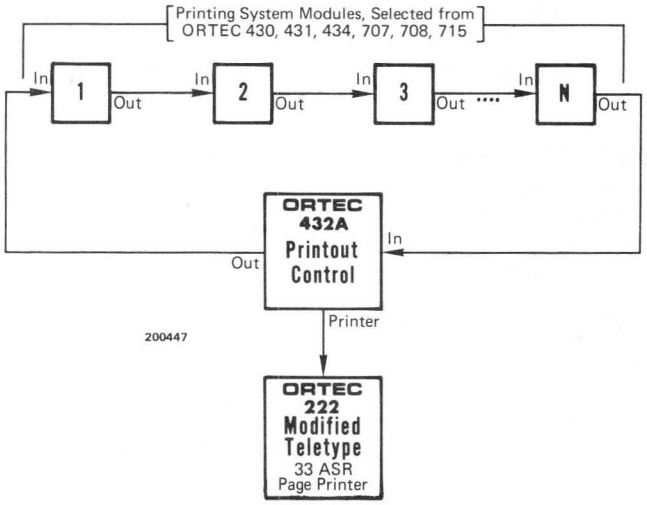


Figure 3.1. Interconnection of Modules for System Operation

3.4 Signal Connections

3.4.1 Counter A INPUT. The signal to be counted by the 715 Counter A can be either polarity. If it is positive or is bipolar with a positive leading edge, it can be furnished through either the front or rear panel BNC, Input A Pos. Since these two connectors are not isolated, signals from two sources should not be connected simultaneously to the two Pos connectors. If the signal is negative or is bipolar with a negative leading edge, it must be furnished through the Input A Neg BNC on the front panel. The input circuit is dc-coupled to eliminate baseline shifts associated with changing counting rates. For signals with an average level greater than ±15 V, use an external capacitive coupling to protect the 715.

3.4.2 Counter B INPUT. The front-panel Input B toggle switch selects either an internally generated Time Base signal or an External signal to be counted. When the switch selects a Time Base, no cabled inputs will be accepted. With this switch on EXT, the characteristics and connections of signals to be counted are identical to those discussed for Counter A above.

3.4.3 GATE Inputs. Gating signals can be applied separately to each counter. GATE B signal will control the Counter B

input signal, whether this is the Internal Time Base or an External signal. Both GATE input signals can be connected to the 715 by either front- or rear-panel-mounted BNC connectors. As in the case of the count input connectors, no isolation is provided between the two inputs associated with one counter, and so two signal sources must not be connected simultaneously to these two inputs. When a GATE input is not connected, the voltage level at the gate connector is about +3 V and the associated counter gate will permit counting. To inhibit counting, this level must be pulled down below +1.5 V but not below -25 V. To do this, the driving circuit must be capable of absorbing 1 mA from the gate input circuit. The gate circuit permits counting when the input voltage level is +3 V or greater but not more than +25 V.

3.4.4 RESET Input. A RESET input signal can be connected to the 715 through the rear-panel BNC connector. To reset either Counter or both to zero, a signal of +3 V or greater originating from zero potential with a minimum width of 100 nsec should be used. The input impedance is greater than 1000Ω. Negative signals will not perform any useful function at the RESET input. The input circuitry will not be harmed by any signal level which does not exceed ±25 V.

3.4.5 OVERFLOW Outputs. An OVERFLOW signal is available through a rear-panel BNC connector for each of the two counters in the 715. A positive signal appears at this output each time that the contents of the corresponding counter reach its maximum capacity. In Counter A the overflow occurs as the count changes from 9 999 999 to 0 000 000. In Counter B it occurs at the change from 999 999 to 000 000. These overflow signals can be used to provide an input to another scaler or counting register, including the alternate counter in the 715. The output signal is a nominal +4-V pulse into a 100Ω load. The output signal width is approximately 2 μsec.

3.4.6 INTERVAL Output. The INTERVAL signal is available through a rear-panel BNC connector. A nominal +3-V level appears at this connector during the time that the 715 is placed in a counting condition. It changes to zero volts when the STOP push button is pressed or a preset condition is reached. This signal is included to permit control of other equipment.

3.4.7 IN/OUT System Connector Signals. The following signals are included in the two 14-pin rear-panel connectors of the 715 and in the connectors of each of the other units designed for use in the printing loop system. All but one of these signals are common to both connectors; the difference is in the signal on pin 7. On the "In" connector, the signal is Previous Module Finished; on the "Out" connector, the signal is This Module Finished. For the functions in the 715, two new control lines are added to those which were previously furnished with all other ORTEC printing digital modules, and they may need to be added to the older control cables if they are involved in the loop connections. Pins 12 and 13, which were previously spare pins, now carry an identification of 432 Off and This Module Printing signal, respectively.

	IN Connector		OUT Connector
Pin	Description	Pin	Description
1	Data 1	1	Data 1
2	Data 2	2	Data 2
3	Data 4	3	Data 4
4	Data 8	4	Data 8
5	Print	5	Print
6	Print Advance	6	Print Advance
7	Previous Module Finished	7	This Module Finished
8	System Gate	8	System Gate
9	System Preset	9	System Preset
10	System Reset	10	System Reset
11	Ground	11	Ground
12	432 Off	12	432 Off
13	Spare	13	Spare
14	This Module Printing	14	This Module Printing

Below is a description of the signals listed above. For more complete information about these signals, see Sections 2 and 5.

Pins 1-4 — Data Lines. Transfer the four bits of each digit from the assigned instrument to the Printout Control. Each instrument includes an isolated program control which drives these common lines only during its turn for printing.

Pin 5 — Print. Prepares the instrument for data transfer during printing.

Pin 6 — Print Advance. Advances the scanner in each instrument for readout of each of its digits during printing.

Pin 7 — Previous Module Finished. Starts the actual data transfer from an instrument when it is its turn to be printed.

Pin 7 — This Module Finished. Is the signal to the next instrument to start its data transfer.

Pin 8 — System Gate. Carries a Gate OFF signal to all instruments set for Slave operation in the system loop. The signal originates in a Master module. When the 715 is set for Slave, the System Gate line will affect both Counter A and Counter B. When the 715 is set for Master, a Gate input to either counter will be imposed on the common System Gate line but will not affect the alternate counter in the 715.

Pin 9 — System Preset. Carries a Preset signal to all modules in the system loop, both Slaves and Masters. Preset condition Gates Off all modules in the system and both counters in a 715. Preset can only originate in Master module, and will be set in a 715 by the first counter in the module to reach its assigned preset condition. If one of the counters (or both) in a Slave 715 reach a Preset condition, it will Gate itself off, without generating a System Preset.

Pin 10 – System Reset. Carries a Reset signal to all modules in the system loop. The signal originates in a Master module or in the 432 or 432A Printout Control. Note that a System Reset signal will complete the function in only the counter(s) that is (are) front-panel-selected in the 715.

Pin 11 – Ground. Carries a common zero potential line to all modules in the system loop.

Pin 12 – 432 Off. Carries an inhibit signal to the Mode control of any 715, disabling the RECYCLE and TEST modes, when there is a 432 or 432A Printout Control included in the system loop with its own Mode switch in any position other than OFF.

Pin 13 – Spare. Cable contains this wire but it is not used.

Pin 14 – This Module Printing. Is grounded only by a 715 Dual Counter/Timer during its printout operation, and signals that a seven-digit unit is being printed.

4. OPERATING INSTRUCTIONS

4.1 Front-Panel Controls

MODE: This three-position toggle switch determines the mode of operation of the 715, unless an ORTEC 432A is connected in the system loop and is turned on, in which case the 715 MODE switch is disabled.

In ONE CYCLE the unit remains gated off after a local preset condition is reached but only as long as no reset signal is applied (manual RESET push button, external RESET signal, or System Reset).

In RECYCLE, when a local preset condition is reached, the unit remains gated off for a given period of time (DWELL TIME), adjustable between 0.3 and 10 sec. After this delay has elapsed, the unit resets itself automatically, as selected by the RESET toggle switch, and returns to the counting mode. If it is set as a MASTER, a System Reset is also generated.

The TEST position applies the internal 60 Hz Time Base fundamental frequency pulses to Counter A and provides the RECYCLE mode.

DISPLAY: Either Counter A or Counter B contents can be monitored at any time except during printout, and the selection is made with this toggle switch. During printout, the display monitors each digit of either counter only during the time it is presented to the common data lines, and the DISPLAY switch has no control.

B INPUT: Is a three-position toggle switch that selects the source of pulses to be counted in Counter B.

The two TIME BASE positions cause internal time base to be counted so that indicators display elapsed time in either 0.1 SEC or 0.1 MIN increments. The start of each counting interval for the 715, when using the TIME BASE for Counter B, is synchronized to the fundamental frequency of the timing circuit.

The EXT position selects input pulses through either the POS or NEG Input B connectors.

COUNT: When this push button is pressed, the unit is set in its counting state.

STOP Push Button: Sets the 715 in the Stop condition. Once this switch is pressed, counting can be resumed only by pressing the COUNT push button.

RESET Push Button: Resets the contents of either one or both counters, according to the position of the RESET toggle switch. Operation of this push button is effective only when the 715 is in either the Stop or the Preset condition, i.e., if the STOP push button has been pressed first or after a local preset condition has been reached.

PRESET A: Two concentric rotary switches permit selection of a count level for Preset in Counter A.

Outer: The outer ring (m) selects Off (in the 0 position) or a significant digit (1 through 9) as a Preset level.

Inner: The inner control (n) selects a power of 10 for the Preset level, from 10^0 through 10^6.

PRESET B: Two concentric rotary switches, same as PRESET A except for an upper limit of 10^5 on the multiplier.

DISC A Screwdriver: This one-turn screwdriver potentiometer provides an adjustment for the threshold level through which a Positive Input signal must rise in order to be counted by Counter A. The threshold level can be adjusted from 250 mV to 5 V.

DISC B Screwdriver: Same as DISC A, for Positive Input to Counter B.

GATE A Indicator: This lamp indicates the condition of Counter A Gating Circuit. The indicator ***on*** means that the counter is enabled to count. The indicator ***off*** means that the counter will not count. When the counter is being gated either on or off at low duty cycles, the neon lamp will not provide a good indication of the gate condition, because the change in light at the gating rate will not be perceptible to the observer.

GATE B Indicator: Same as GATE A Indicator, for Counter B.

OVERFLOW A Indicator: This lamp indicator turns on when Counter A overflows and turns off when Counter A is reset again.

OVERFLOW B Indicator: Same as OVERFLOW A Indicator, for Counter B.

4.2 Rear-Panel Controls

PRINT: This three-position slide switch selects Counter A only, Counter B only, or both A and B for printout. When both are to be recorded, they will be printed in alphabetical order.

MASTER/SLAVE: This two-position slide switch determines the role of the individual module when contained in a counting system as shown in Figure 3-1, with respect to the common System Gate, System Reset, and System Preset signal lines. One or more unit in the system can be selected as the source for these signals by setting this switch as

MASTER. Response to the signals from the System Gate and System Preset lines occurs in the units set at SLAVES, and signals from the System Reset line are accepted by all modules.
In the 715, the two counters are controlled simultaneously by this switch; so both are either MASTERS or SLAVES.

MASTER: A unit selected as MASTER:

1. Turns the System Gate line off when the unit's STOP push button is pressed or when either one of the unit's Gate signals (A or B) is set at ground potential.

2. Transmits a reset signal on the System Reset line when the RESET push button is pressed, when the External Reset input is +3 V minimum, or automatically at the end of each DWELL TIME period if the 715 operates in the RECYCLE mode. Due to the automatic reset feature of the 715, a System Reset is also generated when power is turned on initially or is restored after a power line failure.

3. Is not gated off by a signal on the System Gate line that originated from another MASTER unit. If the System Gate line signal originated locally in either of the counters, the alternate counter is not gated off.

4. Is reset, according to the selection of the RESET toggle switch, by a signal on the System Reset line.

5. Generates a System Preset signal upon reaching the preselected level in either or both counters, and this signal is also effective in both counters in the 715.

6. Is gated off for both counters by a System Preset, which can be generated in any other Master 715 or in any other ORTEC model set for MASTER, SLAVE, or NORMAL.

If more than one MASTER exists in a system, each MASTER will exercise control over the System Gate line. This means that all MASTERS cannot be started by pressing the COUNT push button on any one unit. Instead, each MASTER will have to be started individually.

SLAVE: A unit selected as SLAVE:

1. Does not exercise any output control over the System Gate line.

2. Does not exercise any output control over the System Reset line.

3. Does not exercise any output control over the System Preset line.

4. Is gated off in both counters by a signal on the System Gate line. When one of the local Gate input signals (A or B) is at ground, the corresponding counter is gated off but there is no effect on the alternate counter.

5. Is reset according to the selection of the RESET toggle switch by a signal on the System Reset line or by a local Reset signal.

6. Is gated off in both counters by a System Preset, which can be generated in any Master 715 or in any other ORTEC model set for MASTER, SLAVE, or NORMAL.

4.3 Initial Operation and Test Procedure

1. Insert the 715 into a 401A/402A Bin and Power Supply, or equivalent, with power turned off. Set the RESET toggle switch at A + B and the MODE switch at ONE CYCLE. Then turn power on for the Bin and Power Supply. The unit should reset both counters and then be in the counting state with both Gate indicators on.

2. Press the STOP push button on the 715.

3. Use the DISPLAY selector switch and observe that the contents of both scalers are zero (0 000 000).

4. Set SCALER B switch at 0.1 SEC to count time in 0.1-sec increments.

5. Set Mode switch at TEST and the DWELL TIME vernier at midrange.

6. Set outer ring of PRESET B switch at 1 and inner control of the same switch at 2. The Preset level in Counter B will be 100 counts, or 10.0 sec.

7. Set the outer ring of PRESET A at 0 to turn this function off.

8. Press the COUNT switch, and monitor either counter as desired. Note that both GATE indicators are illuminated while the counters are counting.

9. After 10 sec both GATE indicators turn off and the counters stop counting. The count in Counter B should read 0 000 100. The count in Counter A will read 10 times the fundamental frequency of the Timing circuit; if a 60-Hz power line frequency is used, Counter A should read 0 000 600. After a couple of seconds, both counters should reset automatically, and step 9 repeats indefinitely.

10. Press STOP and RESET push buttons. Set RESET switch at A and press COUNT push button. Same operation as in step 9 should occur, but Counter B should integrate its counts: 0 000 100 at its first reading, 0 000 200 at the second reading, etc. . . . .

11. Repeat step 10, but with RESET switch set at B. This time Counter A should integrate its counts and, if a 60-Hz power line frequency is used, should display successively 0 000 600, 0 001 200, 0 001 800, etc. . . . .

12. Press STOP push button, and reset both counters. Now set the outer ring of PRESET B switch at 0 to turn off this function. Set outer ring of PRESET A switch at 1 and inner control of the same switch at 3. This results in a preset of 1000 counts in Counter A. Press the COUNT push button. When the unit stops counting, Counter A should read 0 001 000 and Counter B should read 0 000 166 (16.6 sec) if a 60-Hz power line frequency is used, or 0 000 200 (20.0 sec) in the case of a 50-Hz power line frequency.

13. Set the 715 front-panel controls as follows:

SCALER B: 0.1 SEC	MODE: ONE CYCLE
PRESET A: OFF ($m = 0$)	DISPLAY: A
PRESET B: $m = 1, n = 2$ (1×10^2)	RESET: A + B

Connect a source of pulses to A INPUT connector which matches its polarity (see Section 2 for Input signal specifications). If using the Positive Input, set the Discriminator Level control for the proper threshold. Push the COUNT push button, and the 715 should count the input pulses. Check to see that the RESET push button has no action unless the STOP push button has been depressed first or a preset condition has been reached. See detailed explanation in 4.4.

14. Ground the GATE A input, and observe that counting stops in Channel A only and the corresponding Gate indicator turns off.

4.4 Operation of the RESET Function and Restart Timing in the ONE CYCLE Mode

4.4.1 Manual Control. To prevent any wrong reading by accidentally pushing the RESET push button during an accumulation interval, a protection circuit is built in the 715 which enables the function of the RESET push button only if the STOP push button has been depressed first or if a Preset condition has been reached.

If the unit is counting, always press the STOP, RESET, and COUNT push buttons in that order. The counters will then start counting again when the COUNT push button is pressed.

If a Preset condition has been reached by either one of the two counters and ONE CYCLE mode is used, the Reset function must be performed prior to starting a new counting period. If the RESET push button is used to that purpose, a slight difference in its effects occurs in the two following situations:

a. Counter B counts externally applied pulses (B INPUT switch on EXT): the counter(s) selected by the RESET toggle switch is (are) reset and both counters start counting at the time the RESET push button is released.

b. Counter B counts the internal Time Base pulses (B INPUT switch on 0.1 MIN or 0.1 SEC): the counter(s) selected by the RESET toggle switch is (are) reset when the push button is depressed; both counters start counting again in synchronism with the first pulse of the Time Base Fundamental Frequency Generator occurring after the RESET push button is released.

Note that when a Preset occurs in the RECYCLE mode the Reset function will be performed automatically when the Dwell Time elapses, even if the unit is reset and restarted manually during that time interval.

4.4.2 Electrical Control: Remote Operation of the Restart. If the scalers have reached a PRESET condition and ONE CYCLE mode is used, it is possible to resume the counting state of the unit by means of an externally applied electrical pulse. All that is needed is to perform the Reset function, which can be done by applying an electrical pulse at the RESET input connector (see specifications in Section 2). In this case, the counter(s) selected by the RESET toggle switch is (are) reset and both counters start counting again:

a. on the trailing edge of the external RESET signal, if B INPUT switch is on EXT,

b. in synchronism with the first pulse of the Time Base Fundamental Frequency Generator occurring after the trailing edge of the external RESET signal, if B INPUT switch is on 0.1 MIN or 0.1 SEC.

Note that the words "trailing edge of the external RESET signal" should be replaced by "approximately 10 μs after the leading edge of the external RESET pulse" if that pulse is shorter than 10 μs.

If several units are connected together in a nonprinting system, it is necessary to apply the external RESET pulse to a Master unit. To achieve full synchronization of the modules connected in the loop, it is recommended that all other units be set as Slaves and that only the Master use its Counter B as a timer. If units other than 715 Dual Counter/Timers are connected in the loop, the external RESET pulse must have a minimum width determined by the unit which requires the widest reset pulse.

4.5 Setup for a Single 715 as a Counter/Timer

Connect the source of pulses to be counted to an A INPUT connector. Set the B INPUT switch at either 0.1 MIN or 0.1 SEC to select an appropriate time base. Set PRESET A if a counting interval is to be stopped at an accumulated count level; set PRESET B if it is to be stopped after a selected elapsed time; or set PRESET A and B if it is to be stopped on the first condition to be met. Select the MODE, ONE CYCLE, or RECYCLE with adjusted DWELL TIME, as desired. Use the RESET toggle to provide either reset of both scalers after each counting interval or integration in one of the scalers. Press the COUNT switch to start counting. Press the STOP switch to terminate the program.

4.6 Setup for 715 as Part of a Counting System

Operate the 715 as a single module, according to the procedure in 4.5 above. Then connect it as a part of a System Loop according to the information in Figure 3-1. If the system data are to be printed automatically with the 432 or 432A Printout Control, the desired printing sequence is a function of the position in the printing loop; set the PRINT switch on the rear panel to determine whether only one scaler or both will be printed out. For a nonprinting system the sequential arrangement of the modules is unimportant, but the system control cables must interconnect all of the modules and a 432 or 432A may be included in the loop and turned off or may be eliminated from the loop.

The MASTER/SLAVE switches of the modules in the system may be set as desired. Normally, one unit is selected as the MASTER, and the remaining units are all set for SLAVE. With this arrangement the entire counting system can be controlled from the MASTER, since its Gate and Reset signals are provided to all of the units. Any MASTER unit in the system can stop system counting by reaching a Preset condition, and this inhibits all units in the system from counting until the System Preset line is released. Any SLAVE 715, reaching a Preset condition, will gate itself off without generating a System Preset to the rest of the units in the counting system.

4.7 Operation as a Frequency Meter

Use the basic setup of 4.5 above, and use PRESET B control settings of 1 for the outer ring and 1 for the inner control; with the B INPUT switch set at 0.1 SEC, the preset time will be 1.0 sec. Provide for reset of Counter A; reset of Counter B is optional. At the end of each 1-sec counting interval the average count rate of pulses into Counter A is available on the Display and/or for printout.

4.8 Operation as a Frequency Ratio Counter

This involves the use of External inputs to both Counter A and Counter B. Either counter may be selected as the base, against which the count rate in the alternate counter is compared, and a preset level should then be selected in the counter used as the base. For example, if Counter A were preset for 10,000 counts (O = 1; • = 4), Counter B would accumulate a significant number of counts per 10,000 counts in Counter A during each counting interval.

4.9 Operation as a High-Capacity Single Scaler

Connect the signal to be counted as the Counter B External Input, and connect the Counter B OVERFLOW output as the Counter A Positive Input. Set the PRESET B controls for Off (O = 0). Preset in Counter A is optional, according to the experiment. There is no internal provision for timing with these connections, but the effective total count capacity is 10^{13}-1 (9 999 999 999 999). Timing control may be furnished as a GATE B input.

4.10 Printing Systems

The 715 Counter/Timer is designed to operate as part of an automatic data acquisition system. Some of the characteristics of its counters and of the printing system are described here, although a more detailed description will be found in the literature describing the ORTEC 432A Printout Control. Counter A in the 715 has a capacity of 7 digits. Counter B has a capacity of only 6 digits. In an ORTEC printing system, provision has been made for the transfer of all digits of data from each scaler.

A rear-panel switch on the 715 permits selection of either Counter A or Counter B, or of both counters, for printout. When both are selected, the program provides for the readout of Counter A, a space, and then Counter B, as if these scalers were included in two separate printing modules. However, the loading effects of the 715 are equivalent to only a single printing module when considering the maximum overall capacity of 50 modules in a system.

The 715, upon command, provides the data stored in its counting registers to the 432 or 432A in a serial-by-character format. The data are fed to the 432 or 432A in groups (characters), one following the other at a rate determined by the 432 or 432A or the printout device. Each group or character is composed of four bits of information in a 1-2-4-8 BCD code, with logic one being about +6 V and logic zero about 0 V. The transfer of data starts with the most significant digit of the counter to be transferred, and proceeds sequentially through the least significant decade. Figure 4-1 shows the sequence of events for a single counting section when it contains the total count 705 849 (assumes six digits from Counter B). As a note of explanation, the Print Command signal originates in the 432 or 432A. It can be initiated either manually, by any module in the printing system reaching a Preset level, or by an external trigger. The Start Data Transfer signal is supplied by the 432 or 432A into module 1 (Figure 3-1), by module 1 into module 2, by module 2 into 3, etc. As each counter finishes transfer of its data, it sends a signal to the next counter in the loop, and is in reality called Previous Module Finished in the 715 schematic diagram.

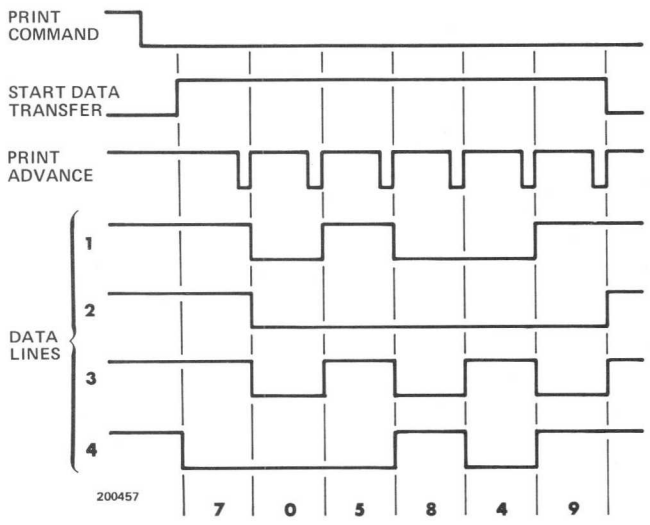


Figure 4.1. Signal Sequence for Transferring Data for 705 839 from a Printing Scaler to the ORTEC 432 or 432A Printout Control

The following sequence of events helps explain how a multiple scaler printing system operates:

1. A Print Command is generated manually, by Preset, or triggered.

2. All counters* and timers stop accumulating and remain static for 1 or 2 sec.

3. All indicators go off except the most significant digit in counter 1, which is printed by the output device.

4. Each of the remaining digits in counter 1 is printed in succession and as each digit is printed the indicator for that digit is illuminated.

5. A space is formed in the printed format after the digits representing the first scaler module.

6. The digits of scaler 2 are printed in succession.

7. A space is formed as in 5.

8. This sequence repeats until the last scaler module has finished printing. The This Module Finished signal to the 432 or 432A indicates completion of the printout cycle.

9. After the last scaler module has been printed one of two basic modes can be selected:

a. The system will remain in a static or noncounting mode until a new cycle is started. The scaler module indicators will be on.

b. A System Reset will be generated and data accumulation will restart.

If this ORTEC 715 Dual Counter/Timer is to be used in a printing system, either with or without additional ORTEC printing modules, some special steps may be required. The exact requirements depend primarily on which model ORTEC Printout Control is to be used, a 432 or a 432A. If a 432 is to be used, again the exact steps will depend upon its serial number. Use whichever set of instructions applies to the combination that is to be used.

To use an ORTEC 432 Printout Control, serial number 176 or lower:

1. In the 432, add a jumper wire between pin 14 of the printing loop connectors marked In and Out on the rear panel.

2. In the 432, add a jumper wire between pin 12 of the printing loop connectors marked In and Out, and also connect this pin 12 circuit to ground by extending the jumper across to pin 11 in either of the connectors.

3. The 715 includes a jumpered connection for the collector of Q11 on its 715-0901 printed circuit board as shown in Fig. 4.2. Remove the jumper wire to restrict the Counter A printout to its six least significant digits and make it compatible with the standard program for the 432 Printout Control. After removing the jumper wire, remove all traces of solder in the through-hole between the two board faces with a #55 drill bit.

4. If any other ORTEC printing modules are included in the system, position the 715 in the printing loop as either the first or the last module. When the system loop cable interconnects the 432 and the 715, the 715 Mode switch is inefffective; remove the cable if the 715 Mode switch is to be used (for example, to select Test).

To use an ORTEC 432 Printout Control, serial number 177 or higher:

1. The 715 includes a jumpered connection for the collector of Q11 on its 715-0901 printed circuit board as shown in Fig. 4.2. Remove the jumper wire to restrict the Counter A printout to its six least significant digits and make it compatible with the standard program for the 432 Printout Control. After removing the jumper wire, remove all traces of solder in the through-hole between the two board faces with a #55 drill bit.

2. If any other ORTEC printing modules are included in the system, position the 715 in the printing loop as either the first or the last module. When the 432 Mode switch is set at Off, the Mode selector in the 715 can be used; with the 432 Mode switch in any other position, the 715 Mode selector is not effective.

To use an ORTEC 432A:

If there are any other ORTEC printing modules in the system, position the 715 in the printing loop as either the first or the last module. When the 432A Mode switch is set at Off, the Mode selector in the 715 can be used; with the 432A Mode switch in any other position, the 715 Mode selector is not effective.

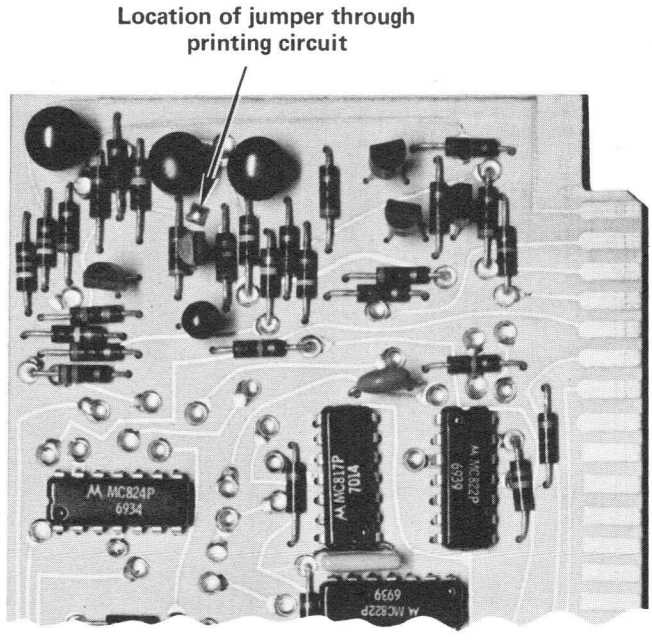


Figure 4.2 Printed Circuit Board 715-0901 for Printout Control

*NOTE: The word Counters is used here to indicate any one of the 400 and 700 Series ORTEC digital printing modules.

5. CIRCUIT DESCRIPTION

5.1 Block Diagram Analysis

The ORTEC 715 Dual Counter/Timer consists mainly of two similar Counting Channels (A and B), a Double Preset Circuit, a Control Logic, a Time Base Generator, and circuits providing the Display and the Printout functions, as shown on the simplified block diagram of Figure 5-1. A detailed block diagram is given in drawing 715-0101-B1. The functions of the various blocks are explained in the following paragraphs.

5.1.1 A Counting Channel. This assembly consists of 5 blocks: an Input Circuit, a Gating Circuit, a 7-decade ripple counter, an Overflow Flip-Flop, and an Overflow Shaper. The Input Circuit accepts either positive or negative signals to be counted, and each path includes a limiter and a discriminator. The outputs of the discriminators are OR'ed to trigger a tunnel diode shaper. The output of this circuit is fed to Counter A through the Gating circuit. This circuit is controlled by an externally applied Gate signal as well as by internal control signals originating from the Control Logic or the System Connector, and lights the Gate A indicator as long as it allows the input pulses to reach the counter. The Counter A block contains 7 decades. Each decade displays its content on four data lines in the BCD Code. The output of the last decade triggers the Overflow A shaper, which delivers the overflow output pulse, and sets the Overflow A Flip-Flop, which turns on the Overflow A indicator.

5.1.2 B Counting Channel. The B Counting Channel closely resembles the A Counting Channel, and the functions described for the previous group of blocks also apply to this one. The major differences are that the Counter B has only 6 decades and that its input is selected from the Input Circuit or the Time Base Generator.

5.1.3 Time Base Generator. This block generates from the timing reference input, which is the line frequency in the basic version of the 715, and is a time base with a period of 0.1 sec or 0.1 min, according to the position of the B INPUT switch.

5.1.4 Readout Scanner. The Readout Scanner, composed of 3 blocks (Sequence Generator, Readout Selector, and Data Gates), provides a sequential scanning of a group of 7 decade scalers for readout. The outputs of each decade of one counter are gated sequentially by the Data Gates onto the common output Data Lines and are furnished to both the Printer Output and the front-panel Display unit. The Sequence Generator provides the required sequential gating signals. During all nonprinting periods, an internal oscillator drives the Sequence Generator for a continuously repeated display of count accumulation, and the Readout Selector selects the counter to be displayed, according to the position of the DISPLAY switch. During each printout cycle, the Sequence Generator is driven by the Print Advance signals from the 432 Printout Control. The Readout Selector is then set by the Printout Control Logic, according to the PRINT switch.

5.1.5 Display. The Display consists of a BCD to Decimal Decoder, 7 H. V. Drivers, and 7 Numerical Indicators. It is of the dynamic type: one single decoder is used to decode 7 decades, in a time sharing mode. The H. V. Drivers, controlled by the Sequence Generator, turn on the Numerical Indicators in synchronism with the scanning of the corresponding decade scalers.

5.1.6 Double Preset Circuit. The Double Preset Circuit is made of 3 blocks: the Preset A Counter, which delivers an output pulse when Counter A reaches a preset condition, as selected by the PRESET A switches; the Preset B Counter, which performs a similar operation for Counter B (PRESET B switches); and a Preset Memory Bistable, which is set by the first of these two output pulses to occur and, by grounding the System Preset line, applies an off condition to the Gating Circuits of both Counting Channels.

5.1.7 Control Logic. The Control Logic essentially consists of a Reset Circuit and a Start-Stop Synchronizing Bistable. The Reset Circuit generates a 10-μs-wide reset pulse, which is fed to the Double Preset Circuit, the Time Base Generator, and the Reset Selector, which opens a path to either one or both Counting Channels as selected by the RESET switch. The Reset Circuit is activated by the RESET push button, a signal applied to a rear-panel connector, or the System Reset line. In the RECYCLE or TEST position of the MODE switch, if the 715 is not connected to an ORTEC 432A Printout Control or is connected to a 432A with its MODE switch in the OFF position, the Reset Circuit is also triggered by a pulse derived by the Delay Generator from the switching transient of the Preset Memory Flip-Flop after a delay adjustable between 0.3 sec and 10 sec by means of the DWELL TIME control. This provides an automatic recycle type of operation. The Delay Generator also generates automatically a trigger pulse for the Reset Circuit when the power is first turned on. The Start-Stop Synchronizing Bistable, which feeds both Gating Circuits, is set or reset by the COUNT and STOP push buttons. Switching of this flip-flop is synchronized by the output pulses of the Fundamental Frequency Shaper when Counter B is used in connection with one of the internal time bases.

5.1.8 Printout Control Logic. The Printout Control Logic interfaces the 715 digital output data lines with the ORTEC 432 or 432A Printout Control to set up a serial-by-character printing system. It also establishes the appropriate sequence for the Readout Selector, according to the setting of the PRINT switch.

5.1.9 Power Supply. The Power Supply produces an unregulated +225 V output to operate the front panel indicators, and a regulated output of +4.8 V to bias the integrated circuits.

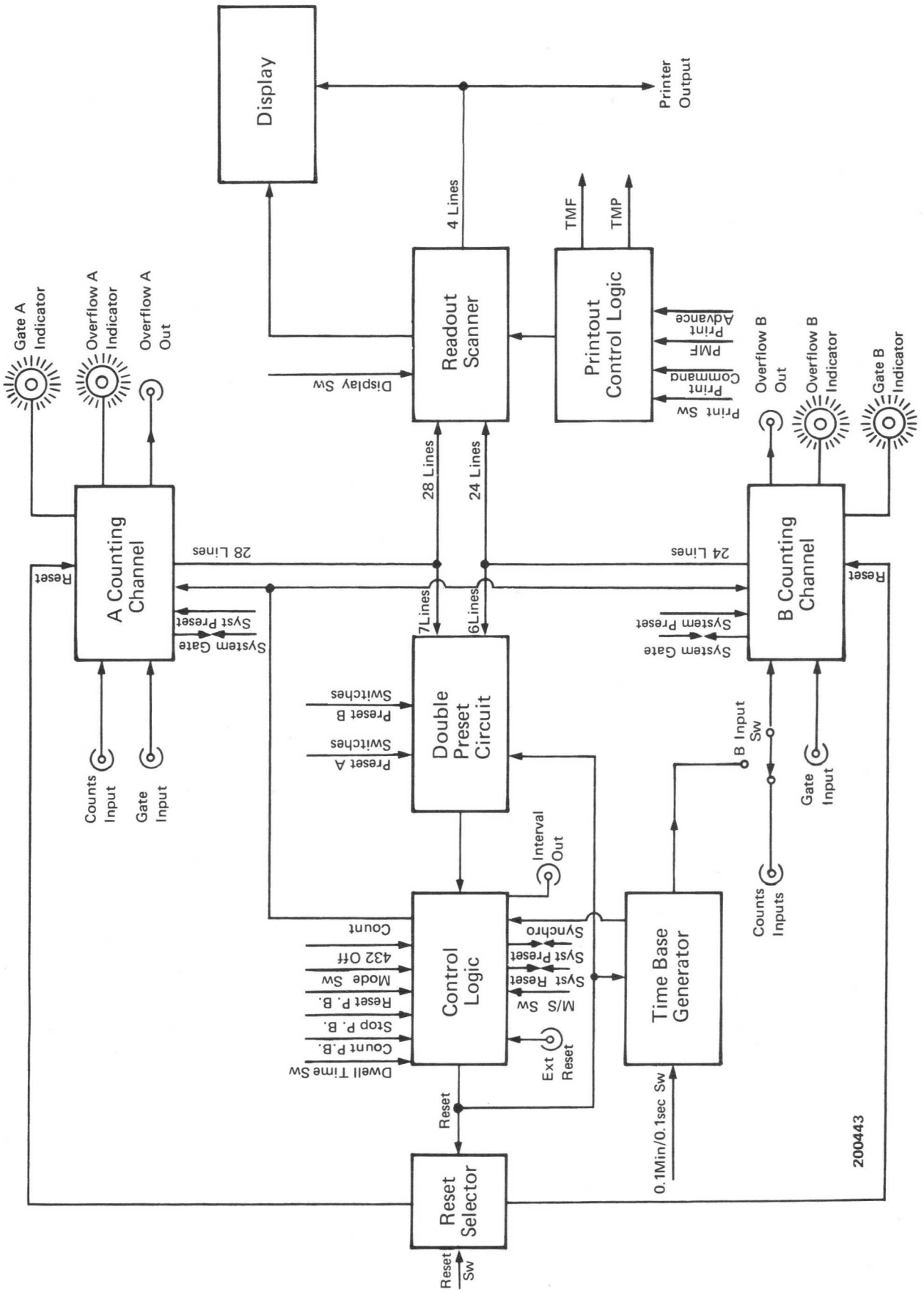


Figure 5.1. Block Diagram of 715 Dual Counter/Timer

5.2 Circuit Analysis

The following circuit analysis describes the operation of the various circuits in detail. A short description of the integrated circuits that are used throughout the 715 Dual Counter/Timer is given at the end of this section. To avoid any ambiguity when an IC package contains more than one circuit, each gate is referred to in the circuit description by the IC number followed by the pin number corresponding to the output of that gate. Unless otherwise specified, all the logic circuits are named by the function that they accomplish in positive logic: a logic "0" is represented by a "low" level, usually the ground potential, a logic "1" being represented by a "high" level, some positive voltage depending on the type of IC used (TTL or RTL).

5.2.1 A Counting Channel. All the circuits of this section are located on Counter A Board (schematic 715-0701-S1).

Input Circuit. The Input Circuit has two separate paths: one for the positive input pulses and one for the negative pulses to be counted. Each path contains a limiter followed by a discriminator. The positive input pulses are first applied to an input protection circuit composed of D8, D9, D10, and their associated resistors. As the input rises toward increasing positive values, the current through R31 is switched progressively to R32, with the result that the base of Q1 follows the input voltage. When the signal increases beyond 6 V, all the current supplied by R30 is routed to R32, and D8 cuts off. At this point the base of Q1 is clamped at about +6 V, so that the emitter to base voltage of Q2 is still below its breakdown value in the worst case (base of Q2 near ground potential). In the case of negative pulses applied to the positive input, D10 clamps the base of Q1 to one junction drop below ground potential, and D9 cuts off as soon as the input voltage is more negative than that value. The variable threshold discriminator consists of a dc-coupled differential amplifier (Q1 and Q2). In the quiescent state, Q1 is off and Q2 is conducting an amount of current determined by the current source Q3. The base of Q2 is connected to a potential adjustable between 0.25 and 5 V. When the input voltage exceeds that value, Q1 is turned on and Q2 is turned off. The current through R36 is then switched to the normally off transistor Q4, which acts as a current driver for the tunnel diode shaper. On the negative signal path, the limiter consists of diodes D4, D5, and D6. As the negative input voltage goes below -4 V, all the current through R23 is supplied by R24, and D4 cuts off, while the base of Q7 is maintained at that potential. For positive input voltages exceeding one junction drop, D5 is turned off and D6 clamps the base of Q7 at +0.7 V. The differential pair Q7 and Q8 is a fixed threshold discriminator, the value of which is determined by the resistive divider R27 and R28 and is adjusted to accept negative inputs greater than -250 mV. In the quiescent state, Q8 is off and Q7 is conducting enough current to bias off the grounded-base transistor Q9 by means of diode D7. When the input signal reaches a negative value greater than -250 mV, Q7 turns off, switching the current normally flowing through it to the emitter of Q9.

The collectors of Q4 and Q9 are connected together, which allows them to drive the same output shaper consisting of a tunnel diode monostable (D11) and a differential amplifier (Q5 and Q6). For short input pulses the tunnel diode one shot delivers an output pulse of approximately 20 nsec. Both the positive and the negative signal paths are dc-coupled from the input up to D11, and the tunnel diode has a dc load line that, for longer pulses, will retain the tunnel diode in its high voltage state after it is triggered until the input signal returns to approximately zero volts. Thus the circuit assures one single count per input pulse, regardless of its width. The differential amplifier (Q5, Q6) provides the voltage swing necessary to drive a TTL logic circuit. The amplified signals are inverted by IC 1- 4 and, with the MODE switch on RECYCLE or ONE CYCLE, are applied to the Gating Circuit through the NAND gate IC 1-13. When the MODE switch is in the TEST position, IC 1-13 is closed and the Gating Circuit is connected by IC 1-10 to the output of the Fundamental Frequency Shaper, which is described in section 5.2.3. The bare collector outputs 10 and 13 of IC 1 are tied together to perform the "wired OR" function.

Gating Circuit. The pulses to be counted are transmitted by gate IC 2 - 6 to the first decade if its input number 5 (Gate A signal) is near ground potential. This happens if all five inputs to the two-level AND function, performed by IC 3, are positive. These signals are COUNT, INHIBIT, and external GATE, applied respectively to inputs 6, 8, and 5 of IC 3, and System Gate and System Preset signals to the second level gate, IC 3-1. The System Gate is connected directly, while System Preset is applied through emitter follower Q15.

COUNT is generated by the Start-Stop Synchronizing Bistable, IC 8-9 on the Preset and Control Logic Board schematic, the operation of which is explained in section 5.2.7. INHIBIT is generated by the Reset Circuit, also located on the Preset and Control Logic Board (IC 5-8). It approaches ground potential as long as any reset action takes place (RESET push button, electrical RESET input, or System Reset) to avoid possible ambiguity resulting from simultaneous application of a count and reset signal to the counter.

The GATE input is followed by a limiter (D1, D2, D3) which performs two functions: it protects the input of the integrated circuit by limiting the voltage at the base of Q10 to +5.5 V for positive input signals, and -0.7 V for negative signals; in the absence of a signal at the GATE input, it raises this point and the base of Q10 to +3 V, to provide input 5 of IC 3 with a logic 1. When the GATE input is grounded, a low level appears at the input of the integrated circuit. Emitter follower Q10 is used as a current switch, capable of sinking the current delivered by the

input of the NAND gate in its low state. The delays in the paths for the signal to be counted, on one hand, and the external gate, on the other hand, compensate each other in such a way that signals applied in perfect synchronism to one of the signal inputs and to the GATE input result in a time difference of only a few nanoseconds at the input of NOR gate IC 2-6.

The System Gate Buffer is located on the Printout Board (transistors Q8 and Q9 of schematic 715-0901-S1). If the 715 is used as a SLAVE unit in the system, a low level on the System Gate line will result, through interfacing transistor Q9, in a low level at pin 2 of IC 3. Either that condition or a zero-volt signal on the System Preset line results in a high level at the output of IC 3-1, which inhibits the counting.

If the 715 is set for Master in the system, the System Gate line is grounded through transistor Q8 of the Printout Board from IC 1-1 as soon as one of its two inputs becomes a logic 0. Input 2 of this gate is connected to the output of gate IC 3-13 of Counter B (see diagram 715-0501-S1), which yields the same logic function on Counter B as does IC 3-13 of Counter A, connected to the second input of gate IC 1-1. The System Gate line is thus driven to ground when either one of the two counters is gated off for any reason other than a System Preset.

When all counting conditions are met, the Gate A signal is low (output of IC 3-1). It is inverted by IC 8-5 of Display (schematic 715-0401-S1) to allow Q18 to conduct and to light the GATE A indicator on the front panel.

Counter A. The first-decade counter (IC 4) is an N8280A integrated circuit, which accepts input pulses at a rate of 20 MHz. The counting operation is performed on the falling edge (negative-going transition) of the input clock pulse: an input signal of long duration will be counted only when the tunnel diode shaper is reset. The six following decades are RTL integrated circuits (IC 5 to 10). The output of each decade is connected to the input of the next one, in a ripple counter arrangement. The Reset line for the six last decades is driven by the buffer IC 11-5, and a reset signal with the correct polarity is furnished to the first decade and the Overflow Flip-Flop by IC 11-3 and IC 2-3.

Overflow Shaper and Overflow Flip-Flop. The output of the last decade is ac-coupled to an univibrator (Q12 and Q13) which is triggered by the negative-going transition. The 2-μs-wide pulse delivered by Q13 is brought to the output connector on the rear panel through emitter follower Q14, and sets the overflow latch consisting of the cross-coupled NOR gates IC 2-11 and IC 2-8 in the position where output 11 is low and 8 is high. This output is connected to the base of the Overflow A indicator driver (Q15 on Display Board), which is then saturated and turns the indicator on.

5.2.2 B Counting Channel. All the circuits involved are located on Counter B board and shown on the corresponding schematic (715-0501-S1). Counting Channel B is very similar to Counting Channel A and the circuit description for Counting Channel A generally applies to Counting Channel B. The two Input Circuits, in particular, show few differences other than circuit symbols. The major differences in the two counting channels are the number of decade counters (6 instead of 7) and the wired-OR gates IC 1-13 and IC 1-10, which are controlled here by the B INPUT switch. With this switch in the EXT position, the input to the Gating Circuit is selected from the output of the pulse shaper (collector of Q5) inverted by IC 1-4, and Counter B is used as a second scaler. In the 0.1 MIN or the 0.1 SEC positions, however, the input to the Gating Circuit receives the pulses from the Time Base Generator, and Counter B plays then the role of a timer.

All inputs to the Gating Circuit, except the electrical GATE input, are shared in common with A Counting Channel, so that the operation of the two counters is totally synchronous except for externally applied GATE signals.

5.2.3 Time Base. The circuits belonging to this functional block are shown in schematic 715-0801-S1 for the Line Frequency Time Base or in 715-1601-S1 for the Crystal Controlled Time Base. These two circuits are directly interchangeable, and either one may be installed in the 715 at any time.

Line Frequency Time Base. The Time Base pulses are derived from the line frequency in the basic version of the 715 Dual Counter/Timer. As the network carries usually a fairly big amount of parasitics, special care must be taken to ensure proper triggering of the shaping circuits. For that purpose the half-wave-rectified signal derived from the Power Supply, first filtered by the low-pass filter R1, C3, R2, with a 3-dB frequency of approximately 600 Hz, drives Q1 into conduction, which in turn triggers the univibrator Q2, Q3. One side of the circuit contains a Darlington "transistor" with an equivalent h_{FE} of at least 5000. This allows the use of a very high resistor in the base circuit (R5, 178KΩ), and a fairly long pulse duration can be achieved with a small size capacitor. This duration is adjusted to 13.5 ms, a value significantly larger than the half period of the line frequency, to keep the circuit from being triggered more than once per cycle. The most critical moment is around the middle of the cycle, when the input signal returns near to ground potential and Q1 comes out of saturation.

The leading edge of the output pulse of the circuit just described triggers the Fundamental Frequency Shaper, a one-shot implemented with two NOR gates (IC 1-5 and IC 1-3), which produces positive pulses of about 1-μs duration. During the accumulation periods (Count signal positive) these pulses are fed through gate IC 2-6 and inverted by IC 1-8, which presents them with the right polarity to the first divider. This circuit is a divide-by-6 for 60-Hz line frequency and is implemented with a decade counter (IC 3), a NAND gate (IC 6-11) connected to the "2" and "4" outputs of the decade, and a one-shot

(iC 7-8, IC 7-5) which is triggered when the NAND gate detects a "6" at the output of the decade and resets it. For 50-Hz line applications the circuit is used as a divide-by-5: a jumper wire permits it to detect a "5" at the output of the decade instead of a 6. The time base of 10 Hz is buffered by two inverters (IC 8-3 and IC 8-5) and applied to the input of Counter B through gate IC 2-3, which is enabled when the B INPUT switch is in the 0.1 SEC position. When this switch is in the 0.1 MIN position, this gate is disabled, whereas gate IC 2-11 opens the way to the 0.1 MIN time base, obtained from the previous one by a division by 10 (IC 4) and by another division by 6 (IC 5, IC 6-3, IC 7-3, and IC 7-14).

The output pulses of the Fundamental Frequency Shaper are also fed to Counter A, in the TEST mode, and to the toggle input of the Start-Stop Synchronizing Bistable, the operation of which will be described in the section "Control Logic." To ensure proper synchronization, the frequency dividers are reset before each accumulation period by the General Reset signal (see "Control Logic"), applied directly to pin 12 of IC 4, and after an inversion by IC 1-14 to the two one-shot circuits through IC 6-8 and IC 6-6 acting as OR circuits. For the same purpose, gate IC 2-6 keeps the output pulses from the Fundamental Frequency Shaper from reaching the frequency dividers as long as the Start-Stop Synchronizing Bistable is in the STOP state (Count signal at zero volts). The INHIBIT signal, disabling gate IC 9-11, prevents them from triggering this bistable as long as a RESET action takes place.

Crystal Controlled Time Base Option. When the optional Crystal Controlled Time Base is installed in the 715 in place of the basic Line Frequency Time Base, the circuit is as shown in schematic 715-1601-S1. The oscillator, Q1 through Q3, operates at 100 kHz and furnishes its output pulses through a countdown circuit for the 0.1-sec and 0.1-min intervals, which can be counted in Counter B. Capacitor C3 is a trimmer that is factory-adjusted for the exact 100-kHz frequency, using a precision reference standard, and should not be changed.

The 100-kHz pulses are gated through IC 1-3, -5, and -8 and IC 2-6 and are furnished as the input to decade IC 10. IC 9-3 and -6 form a buffer to furnish the oscillator output to test point TP1, located on the printed circuit board. The oscillator output is also furnished to Counter A for Test mode operation through IC 9-11 and -8.

The input pulses to decade IC 10 are divided by 1000 through IC 10, IC 11, and IC 12. IC 13 is a flip-flop and provides a 50-Hz output into IC 3. IC 3 is connected as a divide-by-five circuit, and the remainder of this printed circuit operates the same as the alternate Line Frequency Time Base when it is set for a 50-Hz input line frequency.

5.2.4 Readout Scanner. The 715 is equipped with a dynamic type of display, using only one decoder, and is capable of dumping the contents of its Counters on a serial-by-character printer. To do this, it is necessary to send the contents of its decades on a common data bus, one character after the other, on a time-sharing basis. This role is assigned to the Readout Scanner, which consists of Data Gates, a Sequence Generator, and a Readout Selector.

Data Gates. The Data Gates, all located on the same board (schematic 715-0601-S1), consist of 7 groups of 4 NAND gates (IC 1 to IC 7), connected to the BCD outputs of the 7 decades of Counter A, and 6 groups of 4 gates of the same type (IC 9 to IC 14) connected to the outputs of Counter B. All these gates have bare collector outputs, which are tied together to provide an OR function for each BCD common data bus. The four signals are then inverted by IC 8, which drives the Display Decoder (see section 5.2.5) and the Printer Interfacing Gate located on the Printout Board (see section 5.2.8). The four gates of each group have one input tied together and brought to a logic 1 only when the corresponding decade has to be strobed. These control pulses, named G_1 to G_7 for one channel and G'_1 to G'_6 for the other channel, are generated by the two following circuits.

Sequence Generator. The sequence generator is made up of a decade counter followed by a BCD to decimal decoder (IC 2 and IC 3 on Display, drawing 715-0401-S1). The decoder raises sequentially its decimal outputs to a logic 1, at a rate determined by the clock pulses applied to the input (pin 3) of the decade. The decimal outputs "0" to "6" are inverted by 7 NOR gates (IC 5-3 to IC 4-5 on Display schematic) and applied in parallel to the Readout Selector and to the H. V. Drivers. When the decimal "7" output is raised to a positive voltage (pin 2 of IC 3), it triggers a one-shot located on the Printout Board (IC 8-14 and IC 8-3 of drawing 715-0901-S1), the output pulse of which is applied to the Reset input of the decade counter (pin 12 of IC 2). This operation ensures a periodicity of 7 for the sequence generator. As the decimal states "7" through "9" of IC 2 are suppressed, only the three least significant bits of its BCD outputs must be connected to IC 3 for proper decoding. The fourth input of the decoder (2^3) is used for gating purposes. The truth table of its operation shows that input binary codes between "10" and "15" result in all 10 decimal outputs being maintained at zero volts. It suffices then to set the 2^3 input of the decoder to a logic 1 to make sure that none of the 7 outputs of the Sequence Generator are activated. This occurs when both input signals to gate IC 4-8, Display Gate (DG) and This Module Printing (TMP), are at ground potential, which is the case during printout cycles as long as this module is not being printed (explained in detail in section 5.2.8).

During the display intervals the clock pulses that trigger the Sequence Generator are supplied by the Display Oscillator, located on the Printout Board, and made of two NOR gates connected in a free-running multivibrator configuration (IC 2-3 and IC 2-5 on drawing 715-0901-S1). Instead of being connected to a fixed positive voltage, the two pull-up resistors R38 and R39 are fed from the outputs of the

gates through diodes D3 and D4. This prevents the oscillator, from "sticking", which would result if both gate outputs were accidentially at ground potential when the power is first turned on. The frequency of the Display Oscillator is approximately 1 kHz.

Readout Selector. During all nonprinting periods the Display Gate signal, which is generated in the Printout Control Logic, is positive. This allows the dual AND-OR-INVERT circuit IC 1-6 and IC 1-8 to feed either G_1 to G_7 or G'_1 to G'_6 from the 7 output lines of the Sequence Generator, according to the position of the DISPLAY switch. Note that in the second case, where the Data Gate is not enabled during the first scanning step, the Data Lines are then at ground potential, which causes a zero to always be displayed or printed as a first digit for Counter B.

5.2.5 Display. *H. V. Drivers.* As already mentioned, the 7 outputs of the Sequence Generator are also furnished to the H. V. Drivers, Q1 to Q14 on the Display schematic, which switch sequentially the H. V. on the anodes of the seven Nixie tubes. All 7 stages are identical and operate as described here for one of them. Let us assume that at one time IC 3 has a logic 1 on its output pin 3, so that pin 5 of IC 4 approaches ground potential. Q8 turns off and allows the base of Q1 to rise toward 225 V, the value of the H. V. power source. When the voltage at the emitter of Q1 reaches about 170 V, the Nixie tube, the anode of which is tied to that point, ionizes. R2 provides enough base current to bring Q1 into saturation, so that the current through the Nixie tube is limited only by the voltage drop across R1. When the voltage at the output of IC 4-5 becomes positive again, Q8 is switched back into saturation and its collector approaches ground potential. The resistive divider R2 – R3 brings the potential of the base of Q1 down to 100 V, which is far below the ionizing potential, and the Nixie tube is turned off.

Display Decoder. At the same time that one numerical indicator is turned on, the contents of the corresponding decade are gated on the common data lines and are presented to the BCD-to-Decimal Decoder and Driver located on the Decoder Board (schematic 715-1101-S1). The outputs of this integrated circuit have high breakdown voltages, which allow them to drive directly the 10 cathode lines of the Display Unit. The cathode line corresponding to the decimal equivalent of the input to the decoder is grounded, and this number is displayed by the numerical indicator. Diodes D1 to D10 clamp all undriven cathode lines to a prebias voltage of approximately 90 V to eliminate any "glowing" effect on the off cathodes.

5.2.6 Double Preset Circuit. The circuits described in this section are shown on schematic 715-0301-S1 (Preset and Control Logic Board). Preset A operation in the 715 is obtained by means of two switches. The single-pole 7-position Preset A Multiplier Selector provides access to the input of the first decade or the output of the first 6 decades of Counter A. The second switch, a single-pole 10-position switch, called Preset A Digit Selector, determines how many output pulses from the decade selected by the previous switch must be counted by the Preset A Counter before a Preset condition is generated. Actually the output pulses of the selected decade (*n*) are differentiated by C1 - R1 and inverted by IC 5-5, so that their trailing edge toggles the Preset A Counter, consisting of a decade scaler (IC 4) followed by a BCD to decimal decoder (IC 3). The outputs of this circuit are connected to the Digit Selector switch in such a way that, with the switch set on *m*, the NAND gate IC 6-4 is opened after the (*m* - 1) pulse has been counted by IC 4. This allows the *m*th output pulse of the selected decade to trigger the Preset Bistable (IC 6-13, IC 6-10) with as little delay as possible.

The operation of the Preset B circuit is similar. Pins 1 and 4 of IC 6 are tied together to perform the wired OR function. Thus the Preset Bistable is set by the first one of the two Preset Counters to detect a Preset condition. At this time, pin 13 of IC 6 is positive, and the System Preset line is grounded by Q1.

5.2.7 Control Logic and Reset Selector. The Preset and Control Logic Board (diagram 715-0301-S1) contains all the circuits covered by the Control Logic denomination (Delay Generator, Reset Circuit, and Start/Stop Synchronizing Bistable) as well as the Reset Selector.

Delay Generator. If (1) the "432 OFF" line is not grounded and (2) the MODE switch is on TEST or RECYCLE, the NAND gate IC 10-3 has a low level at its output, and the positive-going transition at pin 13 of the Preset Bistable is coupled through C3 to the base of Q4. This p-n-p transistor is then cut off, which removes the emitter saturation current from the normally conducting UJT (Q3) and turns it off. Capacitor C5 is then allowed to become charged, with a time constant depending on the setting of the Dwell Time potentiometer R1. When the voltage across C5 reaches the triggering voltage of the UJT, Q3 turns on again, rapidly discharging C5 and applying a voltage drop to the base of Q4 by means of R22. Q4 is turned on, and brings enough current to the emitter of the UJT to keep it in the saturation mode. The circuit is then again in its stable state. The discharge current of C5 develops a voltage pulse across R10, the delay of which is adjustable by R1 between 0.3 and 10 sec. The delayed pulse is applied through IC 12-3 to the Reset Circuit.

At the end of the Reset operation, Counters A and B start a new accumulation period. This automatic recycle type of operation could lead to conflicts with an ORTEC 432A Printout Control, which has its own Mode Selection switch. Therefore if a 432A is connected to the system and if its MODE switch is in any position other than OFF, the "432 OFF" line is grounded, applying a gate-off condition to IC 11-3 through IC 10-3, regardless of the setting of the MODE switch of the 715, and the automatic recycle operation of the 715 is disabled.

It is important to note that the System Preset line has no action on the Delay Generator. Therefore there is no interference between several units belonging to the same nonprinting system, with different Dwell Time adjustments, even with more than one MASTER. Only that unit which has reached first a Preset can trigger its own Delay Generator and generate a System Reset at the end of this delay.

Automatic Reset. Note that when the power is first turned on or restored after a power line failure, C5 is allowed to become charged and Q3 will be triggered after a certain delay, generating an automatic reset. To keep this delay below 0.5 sec, even with the Dwell Time potentiometer set for the longest delay, R1 is shunted during that initial operation by Q5, which conducts during the charging period of C4.

Reset Circuit and Reset Selector. IC 12-3 and IC 12-5 have their outputs connected together to provide a wired OR function. This point reaches ground potential when a delayed pulse is applied to pin 1 of IC 12 or a positive signal is applied to the Reset connector, producing a positive voltage at pin 7 of IC 12 through the limiter D2, D3, and D4; or when the Reset push button is depressed, setting pin 6 of IC 12 to a logic 1 if IC 12-8 is enabled. This gate is controlled by IC 7-8, which performs an OR function on the output of the Preset Bistable and the STOP signal. Thus the Manual Reset is armed only when a Preset condition has been reached or the STOP push button has been depressed first.

If the 715 is set as a Master, the output of gate IC 12-14 will rise to a positive value and cause Q6 to ground the System Reset line whenever any one of the three previous conditions is fulfilled.

The NAND gate IC 10-11 accomplishes an OR function with negative logic input signals and triggers the Reset Shaper (IC 5-8, IC 8-13) when either one of the three mentioned Reset actions takes place or a zero-voltage level appears on the System Reset line in both the Master and Slave modes. The 10-μs-wide output pulse, called General Reset, resets both Preset Counters, the Preset Bistable, and the frequency dividers of the Time Base and is applied through the Reset Selector (IC 9) to either one or both Counting Channels according to the position of the RESET switch. If Channel B is used as a timer, the General Reset pulse is also applied to the Start/Stop Synchronizing Bistable.

Start/Stop Synchronizing Bistable. The COUNT and STOP push buttons set a memory latch in the corresponding state composed of two cross-coupled NOR gates, IC 7-3 and IC 7-14. An asymmetry is introduced by R16 to ensure that this latch falls automatically into the Count state after a power failure.

The Count/Stop Synchronizing Bistable is a J-K flip-flop (IC 8-9). The synchronous set and clear inputs are fed from the previous latch. One output of this bistable is the count signal which enables accumulation in both counting channels in its high state. Effective switching of this flip-flop occurs only with the first output pulse of the Fundamental Frequency shaper to be applied to its clock input after the state of the memory latch has been changed.

When the B INPUT switch is in the 0.1 MIN or 0.1 SEC position, the General Reset pulse is applied through IC 5-14 to the direct clear input of the Count/Stop Bistable to gate off the two counters, even though the STOP push button has not been depressed. This assures synchronized starting when the unit is operating in a printing system, or in recycle mode in a nonprinting system where the reset signal is the "restart" signal. The Inhibit signal gates off the output of the Fundamental Frequency Shaper (IC 9-11 of Time Base), so that the restart can occur only after the trailing edge of the External Reset pulse or of the System Reset signal or after the Reset push button has been released. When the B Counting Channel is not connected to the internal Time Base (B INPUT switch on EXT), this synchronization is suppressed, and the restart occurs on the trailing edge of the Inhibit signal.

Interval. IC 7-8 and emitter follower Q2 bring the Interval output near ground potential when either a Preset condition or a Stop state is achieved.

5.2.8 Printout Control Logic. The Printout Control circuitry is shown on schematic 715-0901-S1. When a negative Print command from the 432 or 432A is received at the base of Q1, Q2 cuts off and its collector goes positive. This accomplishes three things. First, it causes the Display Gate signal to become zero volts (output of IC 1-5), which gates off the output of the Display Oscillator by means of the NAND gate IC 3-3, enables gate IC 2-8, and, by means of IC 4-8 of Display Board, gates off the outputs of the Sequence Generator, thus keeping all the numerical indicators turned off. Second, it triggers a one-shot (IC 8-8 and IC 1-5), delivering a 100-μs-wide pulse which sets the This Module Ready bistable (IC 5) so that its Q output is low and sets the Printout Selector Bistable (IC 4) in the state corresponding to the first counter to be printed as selected by the PRINT switch. Note that if the printing of both counters is selected Counter A will always be printed first. The Q output of IC 5 (being grounded) sets IC 10-5 to a positive potential which turns Q6 on. With Q6 on, the output from Q7, This Module Finished, is at ground potential. The third action of the Print Command is a delayed action: the output pulse from IC 8-8 is differentiated by C6 and R40 and inverted by IC 9-5, so that the one-shot composed of IC 8-14 and IC 8-3 is triggered on its trailing edge. The 3-μs-wide output pulse of this one-shot resets the Sequence Generator. Since at this time the This Module Finished signal is brought to ground potential in all scalers in the system, the input Previous Module Finished is also at ground potential; therefore the output of IC 1-8, called This Module Printing, is a logic 0, which in turn brings a logic 0 at pin 6 of IC 3 and gates off the interfacing gates IC 6. These gates have

bare collector outputs, so that the four data lines can be pulled to ground potential by any other scaler in the system without interference from this unit.

When the Previous Module Finished signal goes positive, Q4 turns on. The NOR gate IC 1-8 then has its two inputs at a logic 0, and its output (This Module Printing) raises to a logic 1, enabling both the Sequence Generator and the interfacing gates IC 6. At this time the Readout Selector is controlled by the Printout Selector Bistable, the outputs of which are connected to pins 4 and 10 of IC 1 on Display drawing, and the most significant decade of the selected counter is gated onto the common data lines for both display and printout.

To make it possible to insert the 715 in a system containing a standard 6-character-printing 432 Printout Control, provision is made to print only the six least significant decades of both counters. The trailing edge of the pulse which resets the Sequence Generator is differentiated by C8 - R42 and is reshaped by IC 9-14. The IC 1-3, which performs a wired OR function with the output of IC 3-3 and IC 3-11, allows this pulse to be applied to the clock input of the Sequence Generator. Thus, immediately after having been reset, the Sequence Generator skips one position, and the first character to be printed will be the second most significant decade. Gate IC 9-14 is enabled only when the Print Command signal is present, to still allow the display of all 7 digits during all nonprinting periods.

If the printing of all 7 characters of Counter A is desired, a 432A Printout Control must be used, and the action of the circuit just described should be modified by inserting the jumper wire shown in the collector of Q11. After the first digit is printed, the Print Advance signals from the 432 or 432A are then applied through IC 2-8 and IC 3-11 to the clock input of the Sequence Generator, causing it to advance through its sequential selection of decades until the least significant decade has been printed. The next Print Advance signal causes the Sequence Generator to trigger its reset shaper (IC 8-14, IC 8-3), the output pulse of which has two different actions according to the position of the PRINT switch. If only one counter is selected for printout, it is applied to the toggle input of the This Module Ready Bistable (IC 5) and resets it in its initial state. This Module Ready and This Module Printing return to zero volts, whereas the positive-going signal in IC 5-10 will trigger the one-shot bistable made up of IC 10-14 and IC 10-3. This will produce a delay of 80 μs, after which a This Module Finished signal is produced by Q7. If the PRINT switch is in the PRINT A + B position, the output pulse from IC 8-14 causes only the switching of the Selector Bistable IC 4. The toggle input of IC 5 is then connected to the Q output of IC 4. This provides a division by two, allowing the second counter to be printed before This Module Finished is generated.

5.2.9 Power Supply. The Power Supply board (schematic 715-1001-S1) delivers a filtered and regulated voltage of +4.8 V, as well as an unregulated dc voltage of +225 V. A common power transformer, T1, supplies the input power to each of the supplies.

The 117-V ac input power is applied to T1 from the NIM Bin and Power Supply through the power connector on the rear panel of the module. The ac output of one secondary winding is rectified by the full wave bridge rectifier D1 and filtered by capacitors C1 to C3. The voltage regulator circuit consists of a pass transistor Q1, a Zener diode D3 as a reference element, and a one-stage comparator Q2. Potentiometer R2 is set to adjust the output voltage to 4.8 V. This voltage is furnished to all circuits and is called V_{CC1}. It provides the bias for the TTL integrated circuits. The RTL circuits require a lower bias voltage, V_{CC2}, which is obtained on each individual board by one junction drop from V_{CC1}.

The ac output of another secondary winding of T1 is rectified by the full wave bridge rectifier D2 and filtered by capacitor C4. The +225 V output is fed to the H.V. display drivers and the four indicator drivers on the Display board.

5.3 Appendix

5.3.1 Integrated Circuit Description. TTL and RTL integrated circuits are used in the 715. Operating potential at 4.8 V (V_{CC1}) from the Power Supply described in section 5.2.9 is supplied to pin 14 of all TTL packages except type N8T01B, and pin 7 is grounded. The type N8T01B Decoder operates at the same V_{CC1} level connected to pin 16, with pin 8 grounded.

All integrated circuits of the RTL type operate with a V_{CC2} of 4.0 V applied to pin 11, and with ground applied to pin 4.

The logic diagrams of each type of circuit are shown on Figures 5-2 to 5-16. The numbers without parentheses are pin designations, and the numbers in parentheses are loading factors for circuits of the same family.

5.3.2 Wiring Diagram. Wiring diagram 715-0201-S1 is included at the end of this manual to help follow the interconnections between the connectors mounted on the mother board. The connector pin numbers appear in circles on the diagrams of each corresponding printed circuit board to label its input and output lines.

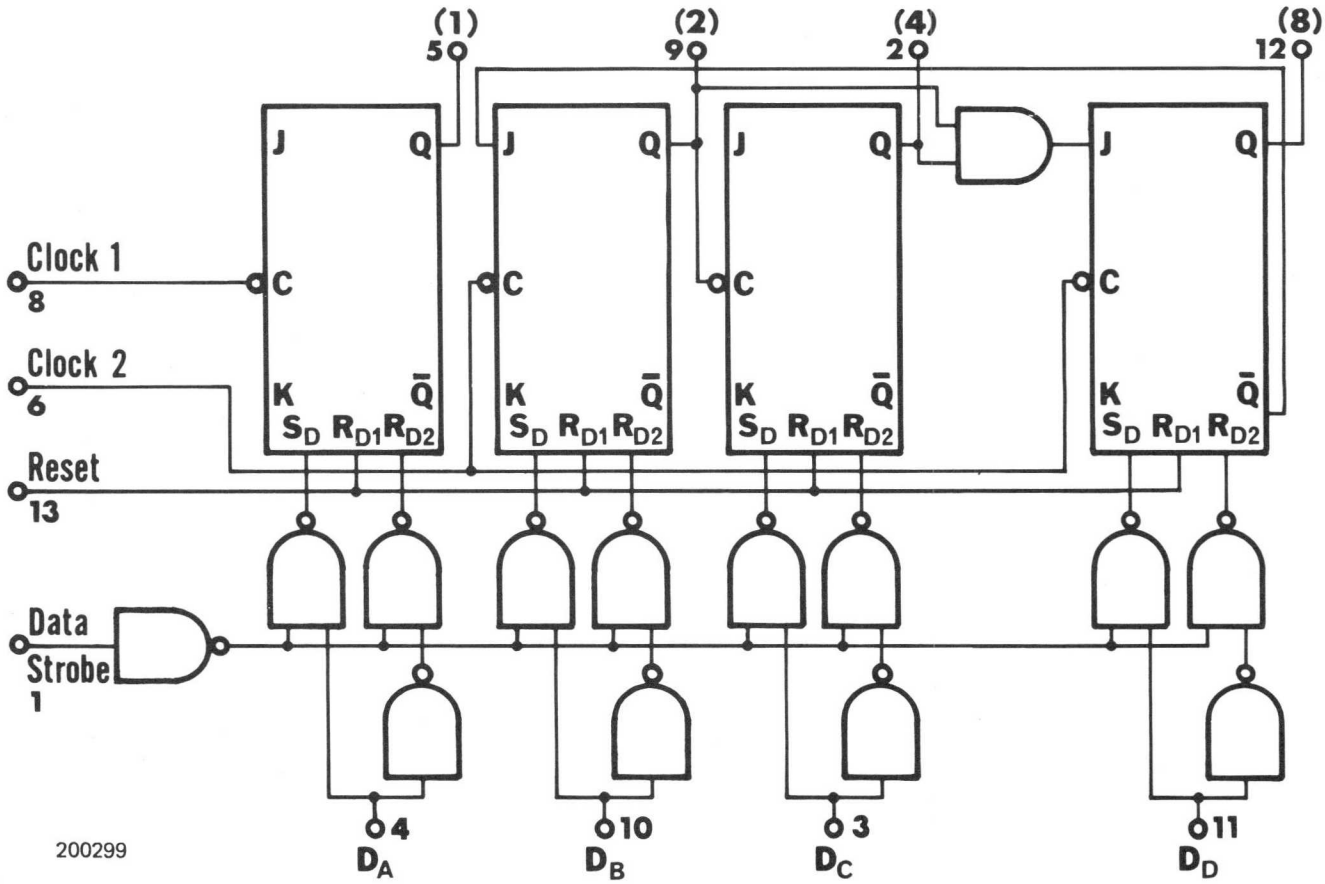


Figure 5.2. TTL N8280A Logic Circuit. Decade Counter/Storage Element

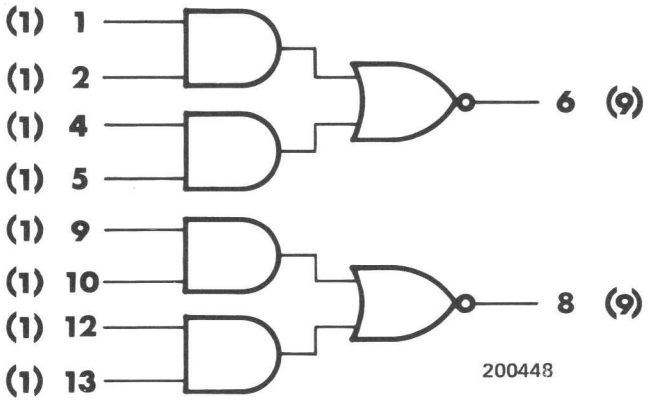


Figure 5.3. TTL N8440A Logic Circuit. Dual And/Or Invert Gate

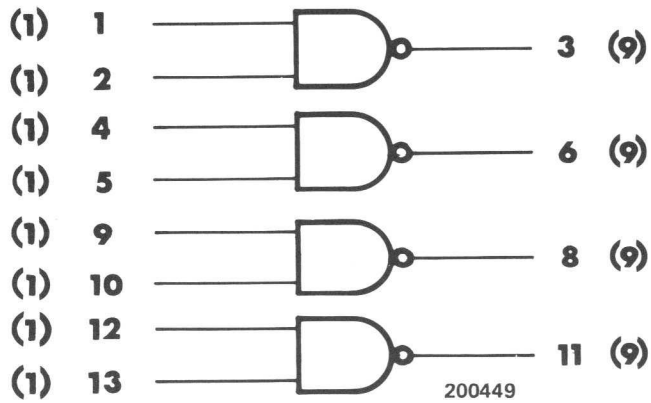


Figure 5.4. TTL N8480A/N8481A Logic Circuit (The N8481A gates have bare output collectors.) Quad 2-Input NAND Gate

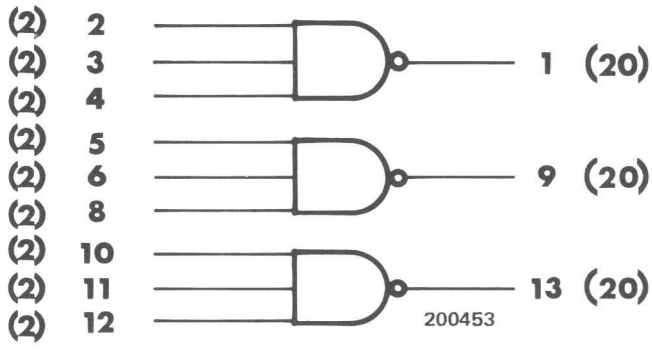


Figure 5.5. TTL N8870A Logic Circuit. Triple 3-Input NAND Gate

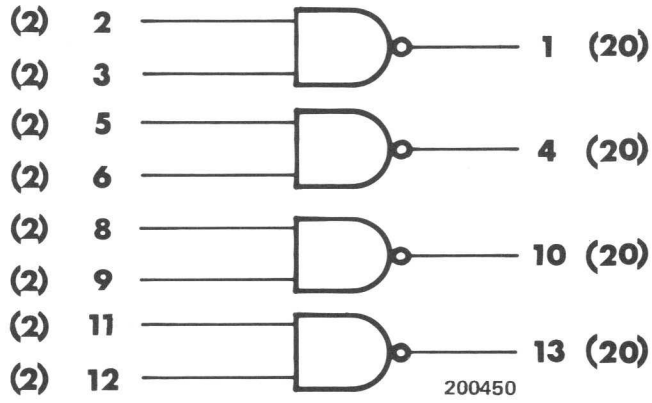


Figure 5.6. TTL N8881A Logic Circuit. Quad 2-Input NAND Gate

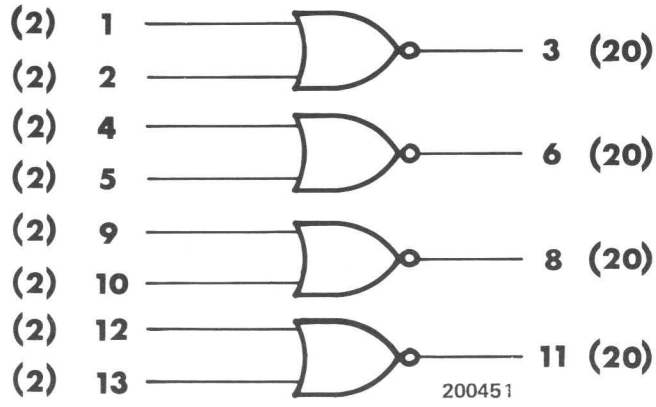


Figure 5.7. TTL N8885A Logic Circuit. Quad 2-Input NOR Gate

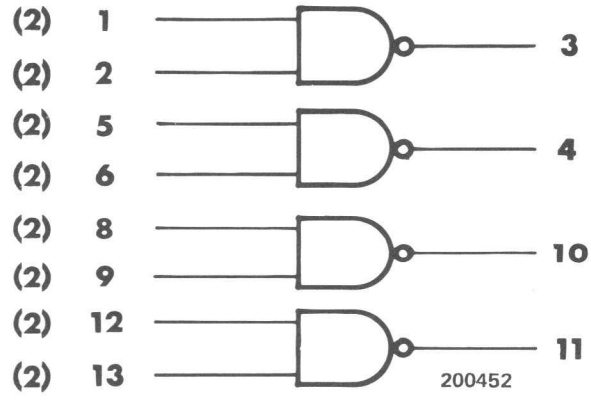
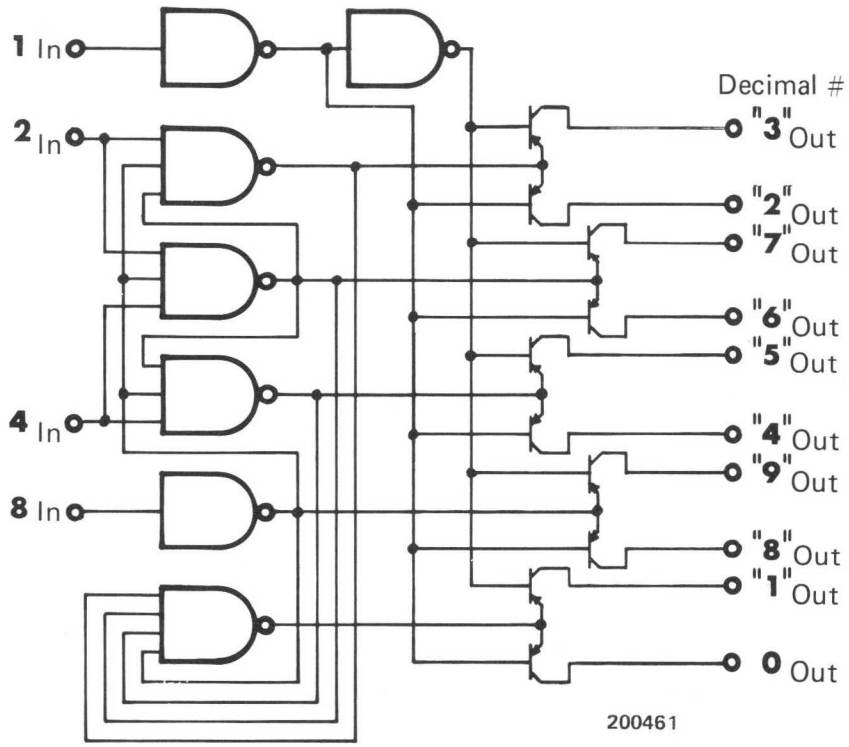


Figure 5.8. TTL N8T80A Logic Circuit. Quad 2-Input NAND Interface Gate



TRUTH TABLE

Input				Output On
8	4	2	1	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	8
1	0	1	1	9
1	1	0	0	8
1	1	0	1	9
1	1	1	0	8
1	1	1	1	9

Figure 5.9. TTL N8T01B Logic Circuit. Nixie Decoder/Driver

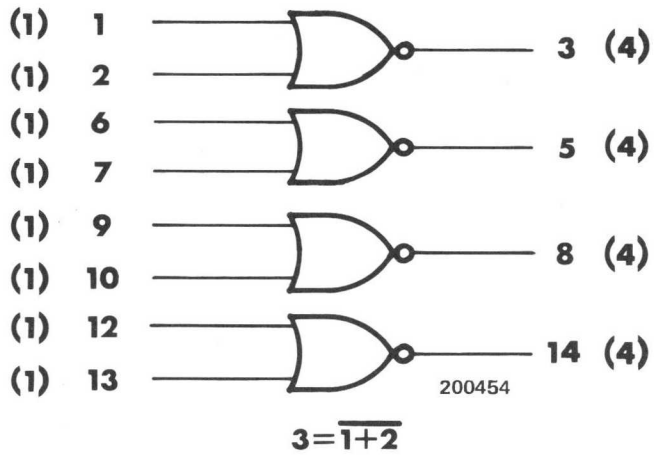


Figure 5.10. RTL MC817P Logic Circuit.
Quad 2-Input NOR Gate

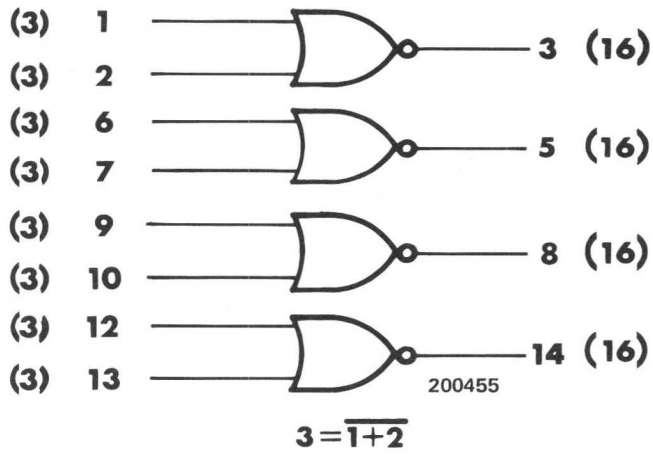
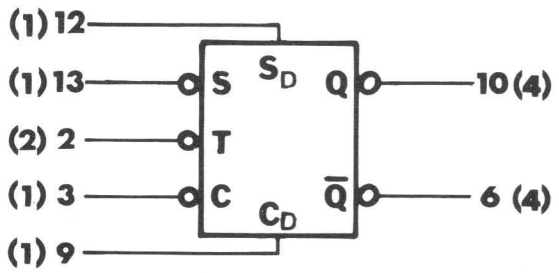


Figure 5.11. RTL MC824P Logic Circuit.
Quad 2-Input NOR Gate



200463

Direct input operation

S_D	C_D	Q	$\overline{Q}$
0	0	—	—
1	0	1	0
0	1	0	1
1	1	0	0

Clocked input operation (S_D and C_D must be low)

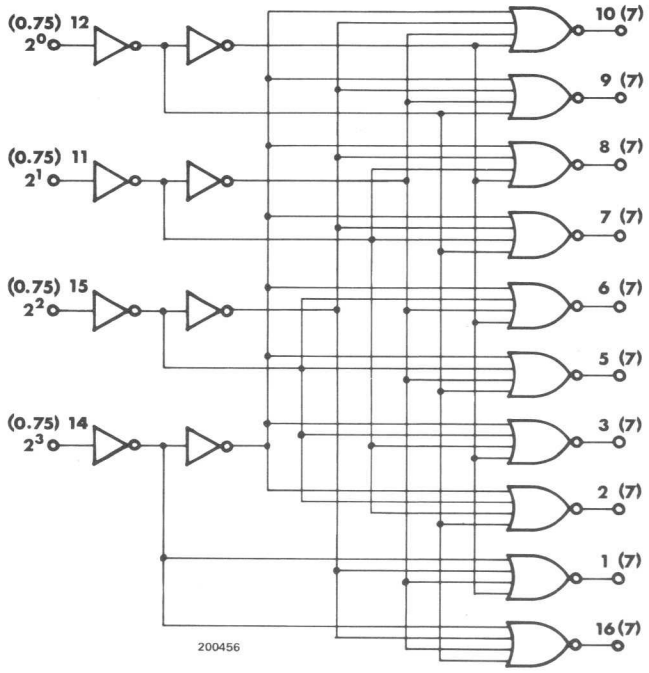
t_n		$t_n + 1$	
S	C	Q	$\overline{Q}$
1	1	Q_n	$\overline{Q_n}$
1	0	1	0
0	1	0	1
0	0	$\overline{Q_n}$	Q_n

t_n = time period prior to negative transition of clock pulse

t_{n+1} = time period subsequent to negative transition of clock pulse

Q_n = state of output in time period t_n.

Figure 5.12. RTL MC822P Logic Circuit. J-K Flip-Flop



200456

TRUTH TABLE

	INPUT (BCD)				OUTPUT (DECIMAL)									
Value	2^3	2^2	2^1	2^0	0	1	2	3	4	5	6	7	8	9
Pin No.	14	15	11	12	10	9	8	7	6	5	3	2	1	16
Logic Level	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	0	0	0	1	0	1	0	0	0	0	0	0	0	0
	0	0	1	0	0	0	1	0	0	0	0	0	0	0
	0	0	1	1	0	0	0	1	0	0	0	0	0	0
	0	1	0	0	0	0	0	0	1	0	0	0	0	0
	0	1	0	1	0	0	0	0	0	1	0	0	0	0
	0	1	1	0	0	0	0	0	0	0	1	0	0	0
	0	1	1	1	0	0	0	0	0	0	0	1	0	0
	1	0	0	0	0	0	0	0	0	0	0	0	1	0
	1	0	0	1	0	0	0	0	0	0	0	0	0	1
	1	0	1	0	0	0	0	0	0	0	0	0	0	0
	1	0	1	1	0	0	0	0	0	0	0	0	0	0
	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	1	1	0	1	0	0	0	0	0	0	0	0	0	0
	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	1	1	1	1	0	0	0	0	0	0	0	0	0	0

Figure 5.13. RTL MC870P BCD-to-Decimal Decoder

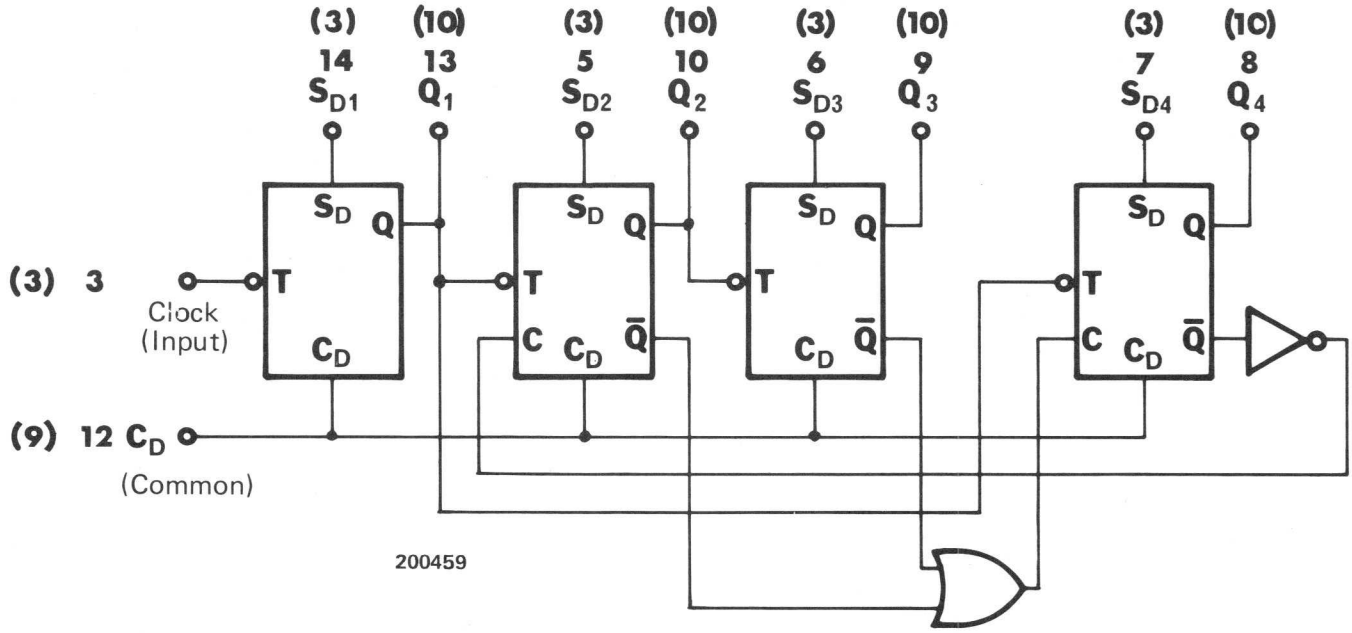
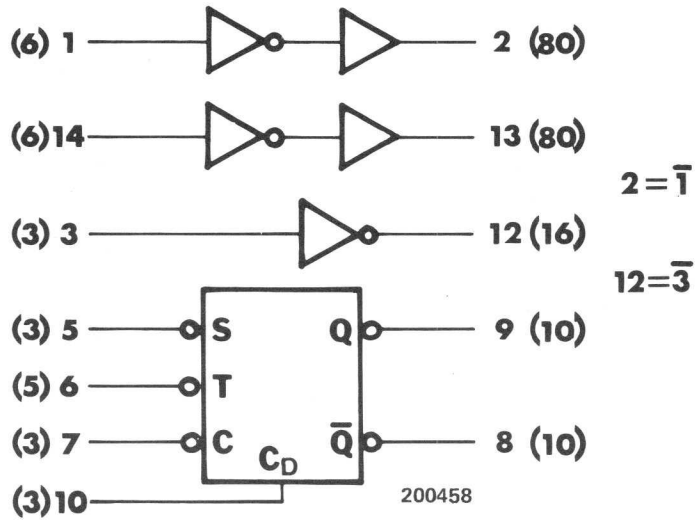


Figure 5.14. RTL MC880P Logic Circuit. Decade Up Counter



Clocked Input Operation
(C_D must be low)

t_n		$t_n + 1$	
S	C	Q	$\overline{Q}$
1	1	Qn	$\overline{Qn}$
1	0	1	0
0	1	0	1
0	0	$\overline{Qn}$	Qn

Figure 5.15. RTL MC887P Logic Circuit. Multifunction Device (1 J-K Flip-Flop, 1 Inverter, 2 Buffers)

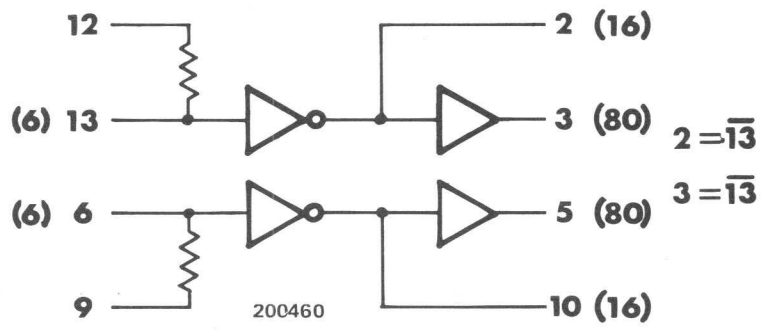


Figure 5.16. RTL MC899P Logic Circuit. Dual Buffer

6. MAINTENANCE INSTRUCTIONS

6.1 Testing Performance

The basic performance of the 715 Dual Counter/Timer can be tested by following the procedure outlined in section 4.3, "Initial Operation." Note that this will not check the unit to its published specifications.

6.2 Calibration Adjustments

There are no calibration adjustments in the 715. There is one jumper wire located on board 715-0801-S1 which determines whether the first frequency divider divides by 5 or by 6, according to the line frequency (50 Hz or 60 Hz).

When the unit is shipped from the factory, its Printout Control Logic is set for operation with a new ORTEC 432A Printout Control, so that all decades of both counters are printed. If printing of only the six least significant digits of Counter A by means of an old 432 is desired, remove the jumper wire from collector of Q11 on Printout Board 715-0901-S1.

6.3 Troubleshooting Suggestions

When a 715 does not function properly, it should first be isolated from all other units. The problem may be in the system interconnection, and isolating the 715 is a quick way to check for improper functioning. Below are listed some of the more common problems that might be encountered, and suggested remedies.

1. Counter A does not count:
   a. Check to see if DISPLAY switch is set on A.
   b. Press in this order: the STOP, RESET, and COUNT push buttons.
   c. Check to see if GATE A indicator is on. If it does not light, go to step f.
   d. If GATE A indicator is on, set MODE switch to TEST. If unit still does not count, IC 1 or IC 2-6 of Counter A is likely bad.
   e. If unit then counts, the problem is most likely in the input circuit. Check if the signal is applied to the right input, according to its polarity. If the positive input is being used, check to see if the discriminator threshold is too high. If a signal of opposite polarity is available, apply to it the other input, after having disconnected the first one. If there is still no counting, check tunnel diode D11 and transistors Q5 and Q6 on Counter A board. If counting is then obtained, trace signal from the other input connector to common collector of Q4 and Q9.
   f. If GATE A indicator is off and cannot be turned on, check to see if GATE B indicator is on. If not, go to step h.
   g. If GATE B is on, the trouble most probably lies with IC 3 of Counter A or with the external GATE input circuit (D1, D2, D3, and Q10). A voltage of approximately +3 V should appear on the GATE input when it is left open-circuited.
   h. If neither of the two GATE indicators lights, check pin 18 of Preset and Control Logic connector for positive pulse of about +2 V, 1 μs duration. This is output signal from Fundamental Frequency Shaper on Time Base board. If signal is present, go to step j.
   i. If signal is not present, check shaping circuit (Q1 to Q3 and IC 1) and output gate (IC 9) on this board, as well as INHIBIT signal (pin 15 of Preset and Control Logic connector) for positive level of about +2 V. If near ground potential, check operation of the Reset circuitry (IC 12, IC 10-11, IC 5-8, and IC 8-13 of Preset and Control Logic) by performing step 9.h.
   j. If the Fundamental Frequency Shaper output pulses are present, check operation of Count/Stop Memory Latch and Count/Stop Bistable (IC 7-3 and -14, IC 8-9 of Preset and Control Logic). Pin 14 of IC 7 should be above +1 V when COUNT push button is pressed, and COUNT signal (pin 9 of IC 8) is about +2 V.
   k. Check pin 10 of IC 8 for logic 0. If voltage at this point exceeds 0.4 V, check IC 8-13, IC 8-2, and IC 5-14.
   l. Check pin L of Counter A Connector for voltage of about +6 V. If voltage at this point approaches zero, check voltage at pin 13 of IC 6 on Preset and Control Logic. If about +0.4 V, check operation of Preset Bistable as in step 11.b.
   m. Check Q 9 on Printout.

2. Counter B does not operate as a scaler:
   a. Check to see if B INPUT switch is on EXT.
   b. Check to see if DISPLAY switch is on B.
   c. Press in this order: the STOP, RESET, and COUNT push buttons.
   d. Check to see if GATE B indicator is on. If not, go to step g.
   e. If GATE B indicator is on, set B INPUT switch to 0.1 SEC. If there is still no counting, IC 1 or IC 2-6 of Counter B is likely bad.
   f. If Counter B then advances at a rate of 10 counts/second, the trouble is most probably in the input circuit of Counting Channel B. Perform the tests that are listed for Channel A under step 1.e.
   g. If GATE B indicator is off and cannot be turned on, check to see if GATE A indicator is on. If not, go to step i.
   h. If GATE A is on, the trouble most probably lies with IC 3 of Counter B or with the external GATE input circuit (D 1, D 2, D 3, Q 10). Check GATE input and base of Q10 for positive voltage of about +3 V.
   i. If neither of the two GATE indicators lights, perform the tests of steps 1.h. through 1.m.

3. Counter B does not operate as a timer:
   a. Follow steps 2.b. through 2.d.
   b. If GATE B indicator is on, set B INPUT switch successively in the two internal time base positions (0.1 SEC and 0.1 MIN). If counting is not observed in these two positions, go to step e.
   c. If counting is observed on 0.1 SEC (10 Hz) but not on 0.1 MIN (1 count every 6 sec), check pin 8 of IC 4 of Time Base for positive 1.6 V, 200-ms-wide signal. Check the operation of IC 6-3 as a divide-by-6, and trace its output signal from this point to pin 11 of IC 2.
   d. If counting is observed on 0.1 MIN but not on 0.1 SEC, check IC 8-3, IC 8-5, and IC 2-3 of Time Base.
   e. If counting is not obtained in either position, check for output pulses from Fundamental Frequency Shaper of about +2 V, 1-μs duration, on pin N of Time Base and perform tests of steps 1.i. and 1.j.
   f. Check the operation of the divide-by-6 (or by-5) IC 3, IC 6, and IC 1 on Time Base.

4. Nixie display does not turn on:
   a. Check GATE indicators. If they do not turn on, the high voltage supply is probably out.
   b. Remove rear-panel In and Out Cables; print signal may be present.
   c. Measure voltage at pin 8 of IC 4 on Display (should not exceed +0.4 V). If above this level, ground this point and see if display unit lights. If this solves the problem, check Q1, Q2, and IC 1-5 of Printout; voltage at pin B of Printout connector should be approximately +3.3 V.

5. One decade not indicated:
   a. Check the corresponding output of the Sequence Generator (IC 4-5, -3, and -14 and IC 5 of Display) for +1.3 V, 1-ms signals at about 150 Hz. If not present, corresponding inverting gate (IC 4, IC 5) or decoder IC 3, or eventually, decade IC 2 is likely bad.
   b. If this signal is present, check corresponding H. V. driving stage (Q1 to Q14 of Display).

6. One decade on, all others off:
   a. Remove rear-panel In and Out Cables to eliminate print-associated signals.
   b. Check pin 5 of Display connector for +1.5 V, 1-kHz square wave. If not present, Display Oscillator (IC 2-3 , IC 2-5 on Printout) is likely bad.
   c. If signal is present, check operation of decade IC 2 on Display. On pin 12 of that integrated circuit, in particular, one should observe 3-μs-wide pulses, at a rate of approximately 150 Hz, riding on a near ground potential baseline. If this is not the case, check the operation of IC 8-14 and IC 8-3 of Printout.

7. Several numerals turn on simultaneously in one display tube:
   a. Check if prebias voltage (pin R of Display connector) is between +80 V and +100 V.
   b. BCD-to-decimal decoder N8T01B or clamping diodes D1 to D10, on Decoder board, may be bad. These circuits are located inside the display base. They can be reached by removing the side cover on the left side of this box and pulling out the whole display assembly.

8. Some numerals of one digit do not turn on:

   The failure is most probably located in the Data Gates associated with this decade. To check this, set DISPLAY switch to the other counter, and see if all numerals of the same display tube then turn on successively.

9. RESET push button is inoperative:
   a. Set MODE switch on ONE CYCLE.
   b. Set DISPLAY and RESET switches in the same position (A for instance).
   c. Press in this order: the STOP and RESET push buttons.
   d. Set now both DISPLAY and RESET switches to the opposite position and repeat step c. If no reset has occurred, neither in step c nor in step d, go to step f.
   e. If reset occurred in one case but not in the other one, check Reset Selector gates (IC 9 of Preset and Control Logic).
   f. If the GATE indicators remain lighted when the STOP push button is pressed, perform the tests of steps 1.h. through 1.j.
   g. If the GATE indicators turn off when the STOP push button is pressed, check IC 7-8, IC 12-8, and IC 12-5 of Preset and Control Logic.
   h. Apply a positive pulse of amplitude greater than 3 V and duration T to the RESET input (rear panel). Check for positive pulses (+1 V), about 10 μs wide, on pin 19 of Preset and Control Logic connector (General Reset signal). The voltage at pin 15 of this connector (INHIBIT signal), normally +2 V, should switch to zero for a duration of 10 μs or T, whichever is greater. Make sure that the System Reset line is not grounded during these tests; voltage at emitter of Q7 should be +5.7 V.

10. Unit will not recycle automatically:
   a. Check to see if MODE switch is on RECYCLE.
   b. If an ORTEC 432A Printout Control is connected in the same system loop, check to see if its MODE is set to OFF.
   c. Set both DISPLAY and RESET switches in the same position (A for instance). Turn off the power switch of the NIM Bin and Power Supply, and then turn it on again while observing the display of the 715 Dual Counter/Timer. An automatic reset should be seen less than 1 sec after the power has been turned on. If this is the case, go to step f.
   d. If the automatic reset does not occur, check operation of manual reset by pressing in this order the STOP and RESET push buttons. If reset did not occur, perform steps 9.g. and 9.h.

e. Check operation of Delay Generator (Q3, Q4, and Q5 on Preset and Control Logic), described in section 5.2.7. If generator does not work, Q3 is then most likely bad.
f. If the automatic reset works, check IC 11-14, IC 11-3, and Q4 on Preset and Control Logic. Q4, normally on, should turn off when Preset Bistable is set (positive-going transient on pin 3 of IC 11) and remain in this state as long as a delayed pulse has not been generated. Check also front-panel potentiometer R1 for open-circuit condition.

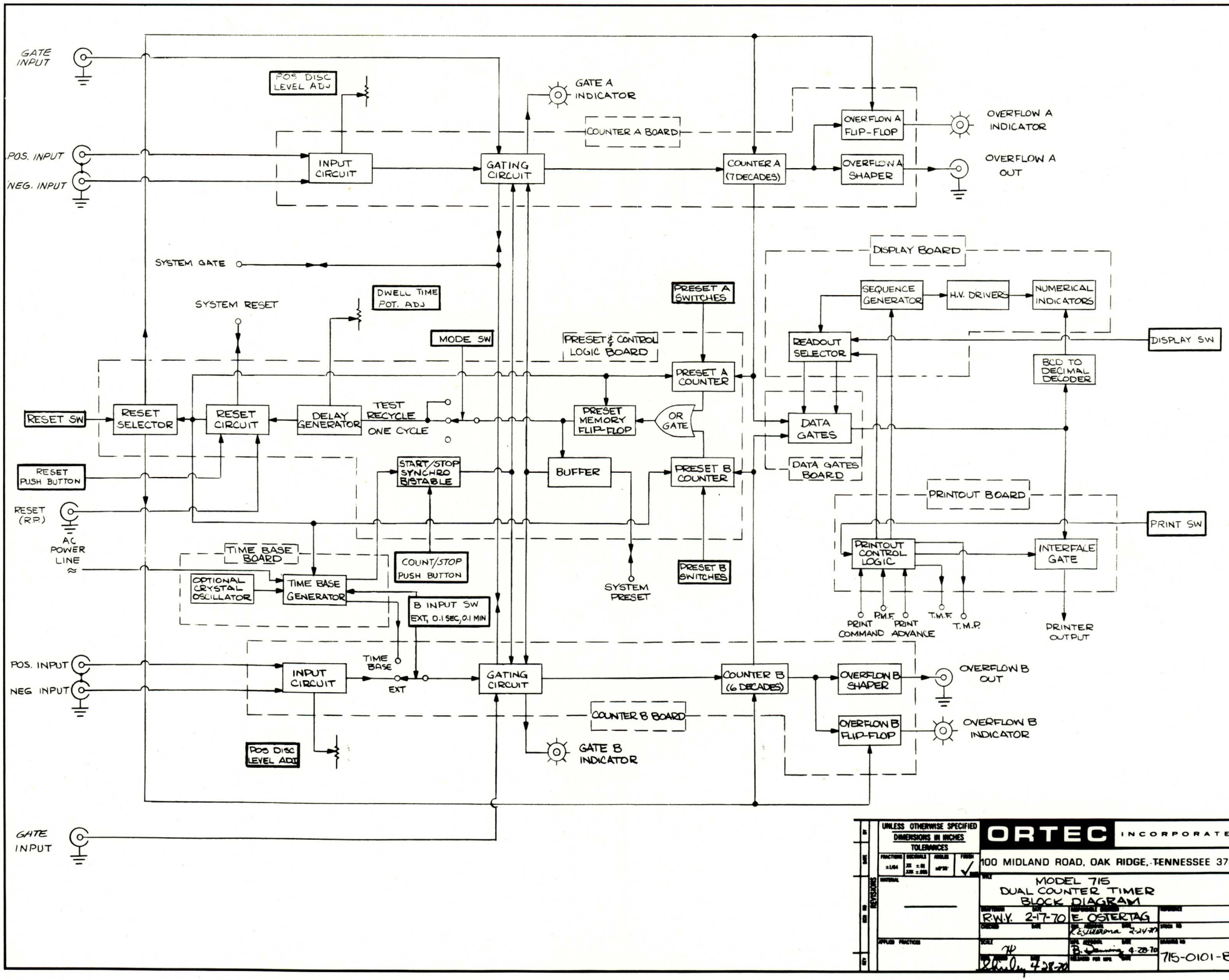
11. Unit will not preset:
a. Check operation of both PRESET A and PRESET B separately, by setting the instrument in, for instance, the TEST mode.
b. If neither operates, check Preset Bistable; in the nonpreset state, check pins 8 and 10 of IC 6 on Preset and Control Logic board for voltages of +4 V and +4.8 V respectively, and pin 13 for approximately zero volts. If voltage at pin 8 is near ground potential, check Reset Circuitry as in step 9.h.
c. If one channel presets but not the other one, check output of IC 5-5 or IC 5-3 for +2 V, 150-ns pulses at a rate equal to that of the output signal of the *n*th decade of corresponding counter (*n* being the setting of Preset Multiplier Selector switch).
d. Check proper operation of decade counter IC 4 (or IC 2) and BCD-to-decimal decoder IC 3 (or IC 1).

12. Printing troubles:
a. Only one counter is printed, although PRINT switch is on A + B. Check IC 4 on Printout Board.
b. Same trouble as in a, and only question marks are printed: This Module Ready bistable is not set when Print Command arrives. Check Q1, Q2, IC 1-5, IC 8-8, and IC 5 on Printout Board.
c. Both counters are printed when PRINT switch is on A + B, but only question marks are printed: check IC 3-8, IC 1-8, IC 2-14, IC 3-6, and IC 6.
d. Printing does not start with the first (or the second) digit: check IC 9-5, IC 8-5 on Printout Board.

BIN/MODULE CONNECTOR PIN ASSIGNMENTS FOR AEC STANDARD NUCLEAR INSTRUMENT MODULES PER TID-20893

Pin	Function	Pin	Function
1	+3 volts	23	Reserved
2	-3 volts	24	Reserved
3	Spare Bus	25	Reserved
4	Reserved Bus	26	Spare
5	Coaxial	27	Spare
6	Coaxial	*28	+24 volts
7	Coaxial	*29	-24 volts
8	200 volts dc	30	Spare Bus
9	Spare	31	Spare
*10	+6 volts	32	Spare
*11	-6 volts	*33	115 volts ac (Hot)
12	Reserved Bus	*34	Power Return Ground
13	Spare	35	Reset
14	Spare	36	Gate
15	Reserved	37	Spare
*16	+12 volts	38	Coaxial
*17	-12 volts	39	Coaxial
18	Spare Bus	40	Coaxial
19	Reserved Bus	*41	115 volts ac (Neut.)
20	Spare	*42	High Quality Ground
21	Spare	G	Ground Guide Pin
22	Reserved		

**These pins are installed and wired in parallel in the ORTEC 401A and 401B Modular System Bins.*

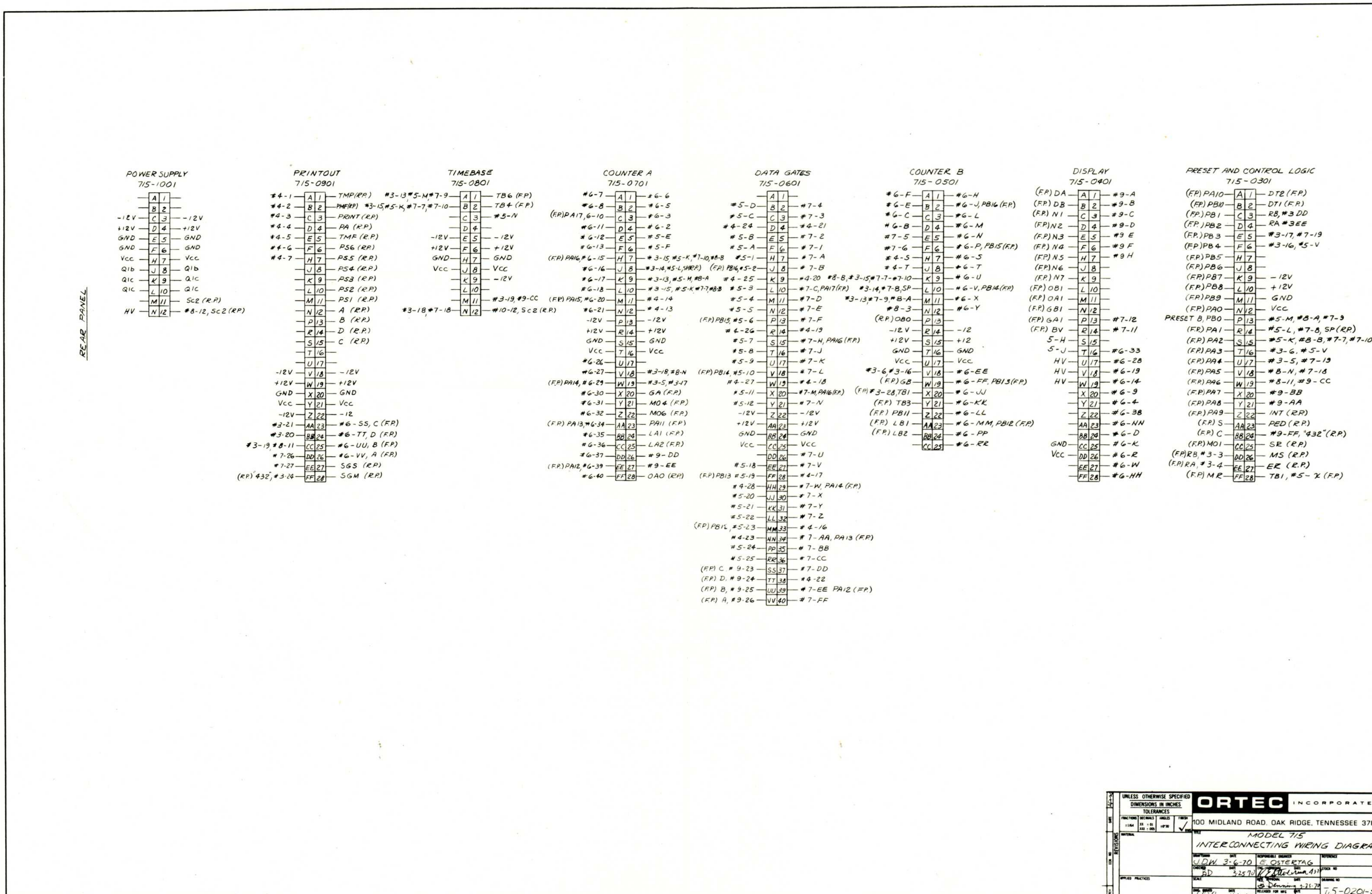


UNLESS OTHERWISE SPECIFIED
DIMENSIONS IN INCHES
TOLERANCES
FRACTIONS ±1/64 | DECIMALS .XX ±.01, .XXX ±.005 | ANGLES ±0°30' | FINISH
MATERIAL —
APPLIED PRACTICES

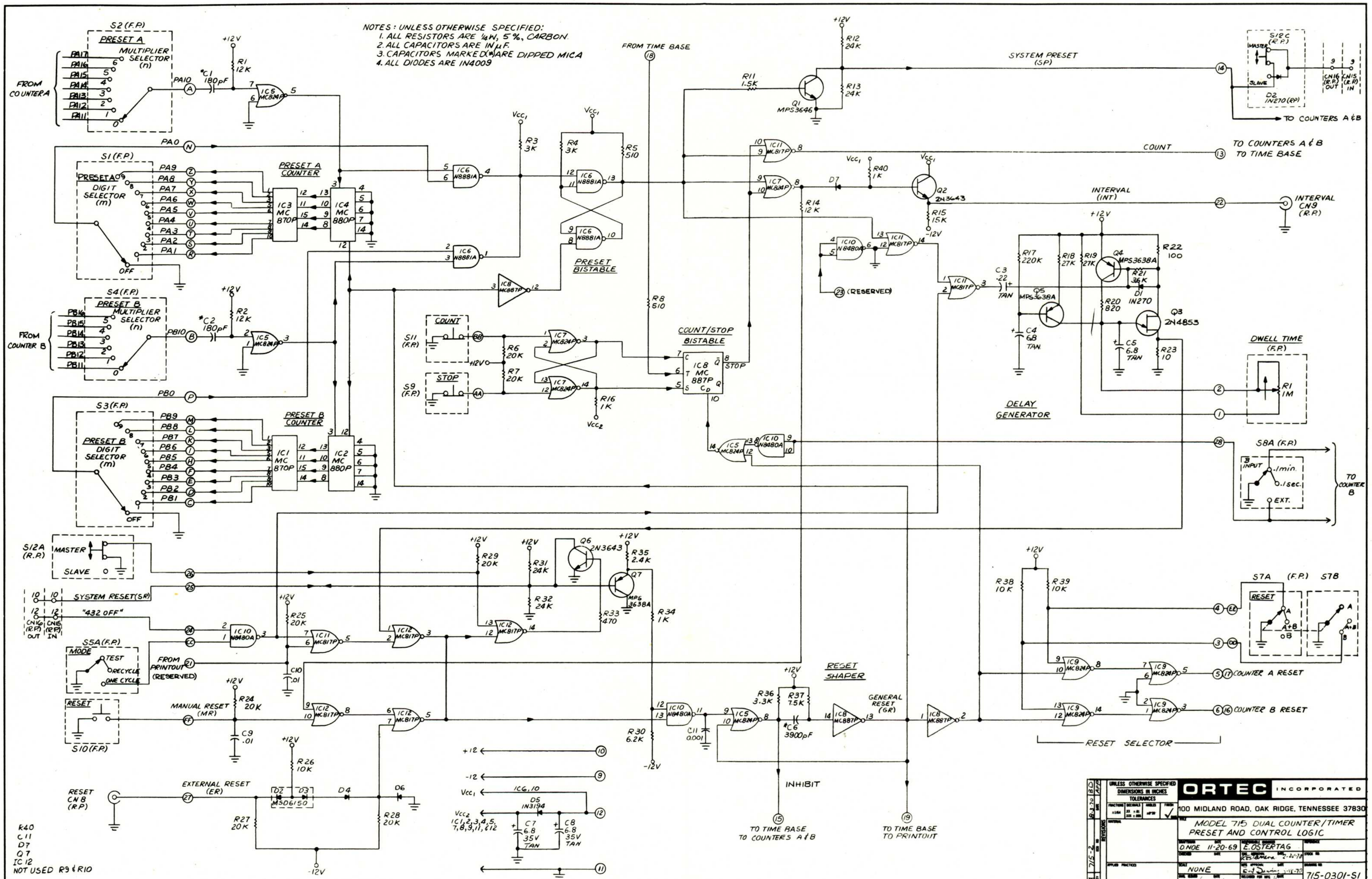
ORTEC INCORPORATED
100 MIDLAND ROAD, OAK RIDGE, TENNESSEE 37830

TITLE: MODEL 715 DUAL COUNTER TIMER BLOCK DIAGRAM

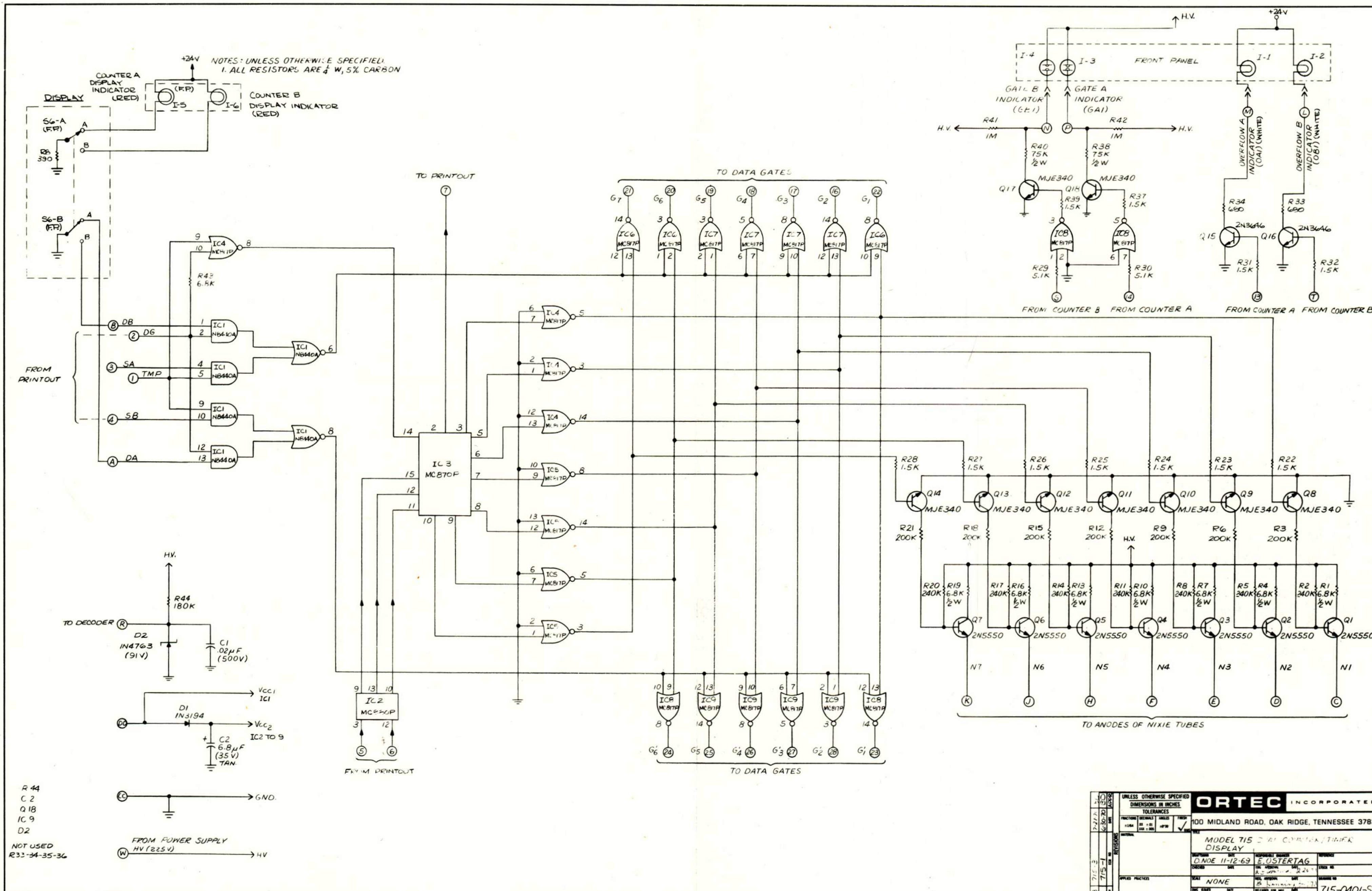
DRAWN R.W.V. 2-17-70	ENGINEER E. OSTERTAG		REFERENCE
CHECKED	ENG. APPROVAL 2-24-70		STOCK NO
SCALE NONE	QUALITY APPROVAL 2-28-70		DRAWING NO 715-0101-B1
ENGINEER APPROVAL 4-28-70	RELEASED FOR DATE		


POWER SUPPLY
715-1001
PRINTOUT
715-0901
TIMEBASE
715-0801
COUNTER A
715-0701
DATA GATES
715-0601
COUNTER B
715-0501
DISPLAY
715-0401
PRESET AND CONTROL LOGIC
715-0301
REAR PANEL
FRONT PANEL
UNLESS OTHERWISE SPECIFIED
DIMENSIONS IN INCHES
TOLERANCES
ORTEC INCORPORATED
100 MIDLAND ROAD, OAK RIDGE, TENNESSEE 37830
MODEL 715
INTERCONNECTING WIRING DIAGRAM
J.D.W. 3-6-70
E. OSTERTAG
715-0201-S1

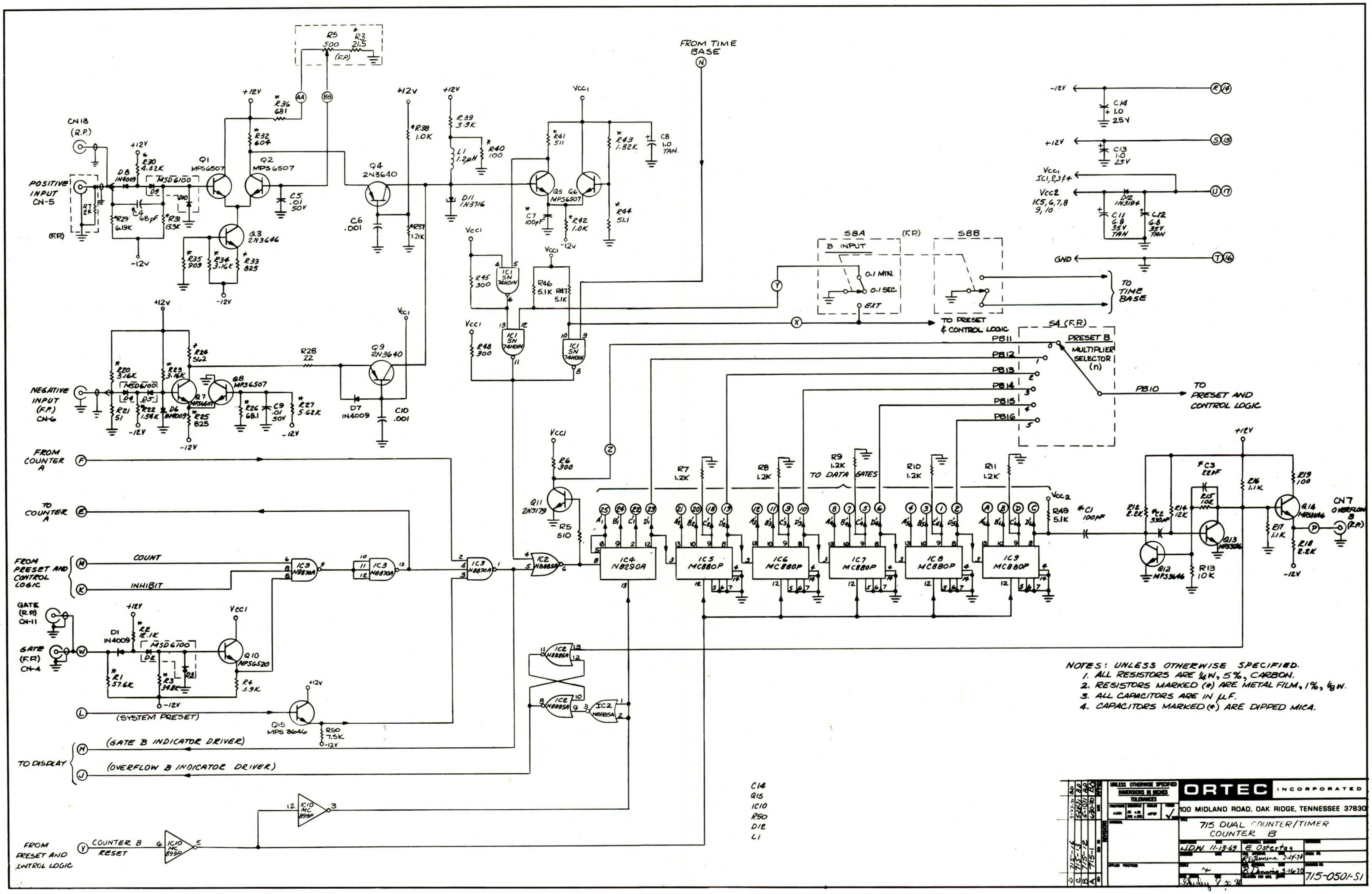
The transistor types installed in your instrument may differ from those shown in the schematic diagram. In such cases, necessary replacements can be made with either the type shown in the diagram or the type actually used in the instrument.


NOTES: UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTORS ARE ¼W, 5%, CARBON.
2. ALL CAPACITORS ARE IN μF.
3. CAPACITORS MARKED (*) ARE DIPPED MICA
4. ALL DIODES ARE IN4009
PRESET A COUNTER
PRESET B COUNTER
PRESET BISTABLE
COUNT/STOP BISTABLE
SYSTEM PRESET (SP)
COUNT
INTERVAL (INT)
DELAY GENERATOR
DWELL TIME (F.P.)
RESET SHAPER
GENERAL RESET (GR)
RESET SELECTOR
COUNTER A RESET
COUNTER B RESET
TO TIME BASE TO COUNTERS A & B
TO TIME BASE TO PRINTOUT
INHIBIT
NOT USED R9 & R10
UNLESS OTHERWISE SPECIFIED DIMENSIONS IN INCHES TOLERANCES
ORTEC INCORPORATED
100 MIDLAND ROAD, OAK RIDGE, TENNESSEE 37830
MODEL 715 DUAL COUNTER/TIMER
PRESET AND CONTROL LOGIC
D. NOE 11-20-69
E. OSTERTAG
NONE
715-0301-S1

The transistor types installed in your instrument may differ from those shown in the schematic diagram. In such cases, necessary replacements can be made with either the type shown in the diagram or the type actually used in the instrument.


NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE ¼ W, 5% CARBON
DISPLAY
COUNTER A DISPLAY INDICATOR (RED)
COUNTER B DISPLAY INDICATOR (RED)
S6-A (F.P.)
S6-B (F.P.)
R8 390
TO PRINTOUT
FROM PRINTOUT
TO DATA GATES
FRONT PANEL
GATE B INDICATOR (GBI)
GATE A INDICATOR (GAI)
OVERFLOW A INDICATOR (OAI) (WHITE)
OVERFLOW B INDICATOR (OBI) (WHITE)
FROM COUNTER B
FROM COUNTER A
TO ANODES OF NIXIE TUBES
TO DECODER
FROM POWER SUPPLY HV (225V)
R44 C2 Q18 IC9 D2 NOT USED
R33-34-35-36
ORTEC INCORPORATED
100 MIDLAND ROAD, OAK RIDGE, TENNESSEE 37830
UNLESS OTHERWISE SPECIFIED
DIMENSIONS IN INCHES
TOLERANCES
MODEL 715 DUAL COUNTER/TIMER DISPLAY
D.NOE 11-12-69
E. OSTERTAG
SCALE NONE
715-0401-S1

The transistor types installed in your instrument may differ from those shown in the schematic diagram. In such cases, necessary replacements can be made with either the type shown in the diagram or the type actually used in the instrument.


FROM TIME BASE
POSITIVE INPUT CN-5
CN13 (R.P.)
NEGATIVE INPUT (F.P.) CN-6
FROM COUNTER A
TO COUNTER A
FROM PRESET AND CONTROL LOGIC
COUNT
INHIBIT
GATE (R.P.) CN-11
GATE (F.P.) CN-4
(SYSTEM PRESET)
(GATE B INDICATOR DRIVER)
(OVERFLOW B INDICATOR DRIVER)
TO DISPLAY
COUNTER B RESET
TO PRESET & CONTROL LOGIC
TO TIME BASE
S8A (F.P.) S8B
B INPUT
0.1 MIN.
0.1 SEC.
EXT
S4 (F.P.)
PRESET B MULTIPLIER SELECTOR (n)
TO PRESET AND CONTROL LOGIC
TO DATA GATES
CN7 OVERFLOW B (R.P.)
IC4 N8290A
IC5 MC880P
IC6 MC880P
IC7 MC880P
IC8 MC880P
IC9 MC880P
NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL RESISTORS ARE ¼W, 5%, CARBON.
2. RESISTORS MARKED (*) ARE METAL FILM, 1%, ⅛W.
3. ALL CAPACITORS ARE IN µF.
4. CAPACITORS MARKED (*) ARE DIPPED MICA.
C14
Q15
IC10
R50
D12
L1
ORTEC INCORPORATED
100 MIDLAND ROAD, OAK RIDGE, TENNESSEE 37830
715 DUAL COUNTER/TIMER
COUNTER B
J.D.W. 11-13-69
E. Ostertag
715-0501-S1

FROM DISPLAY

FROM COUNTER A

FROM COUNTER B

V_{CC1}

R1 1.5K
R2 1.5K
R3 1.5K
R4 1.5K

IC1 IC2 IC3 IC4 IC5 IC6 IC7 IC8 IC9 IC10 IC11 IC12 IC13 IC14

IC8 NB480A

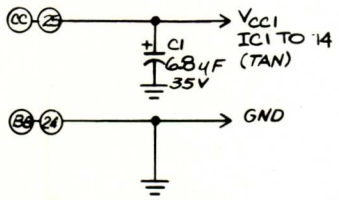
$\overline{A}$ $\overline{B}$ $\overline{C}$ $\overline{D}$

TO DECODER, TO PRINTOUT

FROM DISPLAY

R4
C1
IC14

NOTES:
UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE ¼W, 5% CARBON
2. ALL IC'S ARE N8481A



UNLESS OTHERWISE SPECIFIED
DIMENSIONS IN INCHES
TOLERANCES

ORTEC INCORPORATED
100 MIDLAND ROAD, OAK RIDGE, TENNESSEE 37830

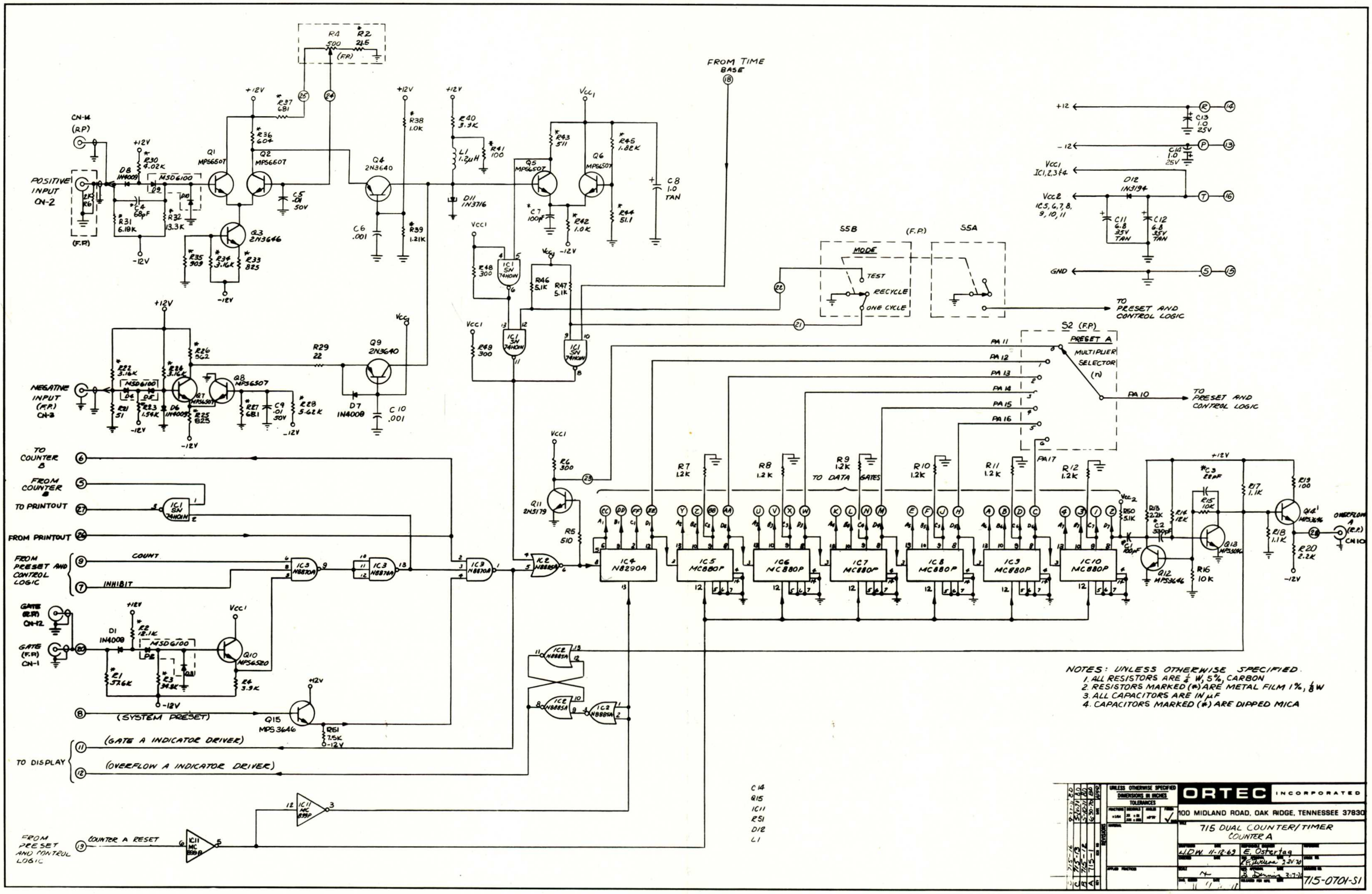
MODEL 715 DUAL COUNTER/TIMER
DATA GATES

DC 10-16-69 E. OSTERTAG
B. Dennis 4-28-70

715-0601-51

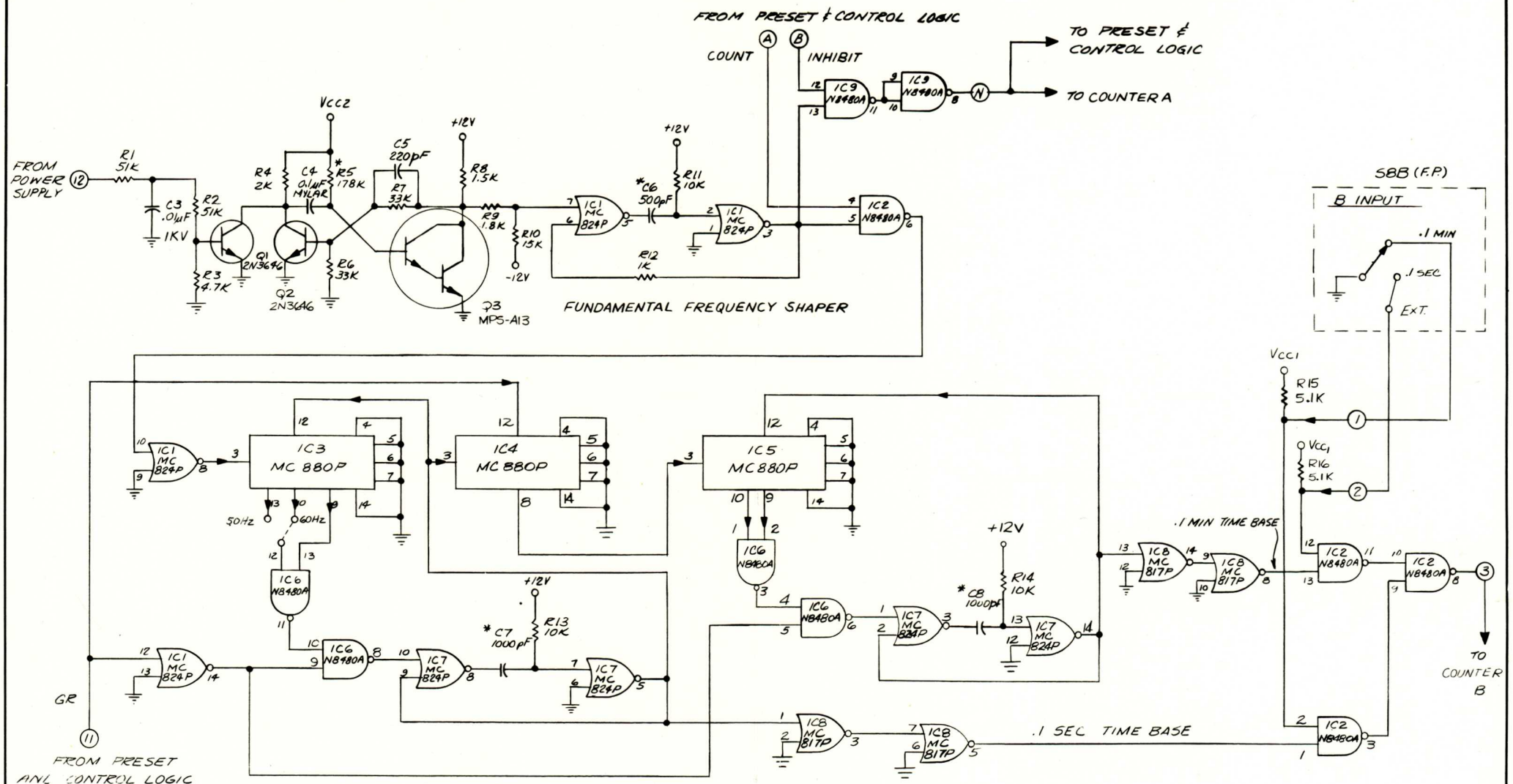
A 715

The transistor types installed in your instrument may differ from those shown in the schematic diagram. In such cases, necessary replacements can be made with either the type shown in the diagram or the type actually used in the instrument.



POSITIVE INPUT CN-2
NEGATIVE INPUT (F.P.) CN-3
FROM TIME BASE
TO COUNTER B
FROM COUNTER B
TO PRINTOUT
FROM PRINTOUT
FROM PRESET AND CONTROL LOGIC
COUNT
INHIBIT
(SYSTEM PRESET)
(GATE A INDICATOR DRIVER)
(OVERFLOW A INDICATOR DRIVER)
TO DISPLAY
COUNTER A RESET
TO PRESET AND CONTROL LOGIC
PRESET A
MULTIPLIER SELECTOR (n)
MODE
TEST
RECYCLE
ONE CYCLE
TO DATA GATES
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE ¼ W, 5%, CARBON
2. RESISTORS MARKED (*) ARE METAL FILM 1%, ⅛W
3. ALL CAPACITORS ARE IN µF
4. CAPACITORS MARKED (#) ARE DIPPED MICA
ORTEC INCORPORATED
100 MIDLAND ROAD, OAK RIDGE, TENNESSEE 37830
715 DUAL COUNTER/TIMER
COUNTER A
W.D.W. 11-12-69
E. Ostertag
715-0701-S1

The transistor types installed in your instrument may differ from those shown in the schematic diagram. In such cases, necessary replacements can be made with either the type shown in the diagram or the type actually used in the instrument.

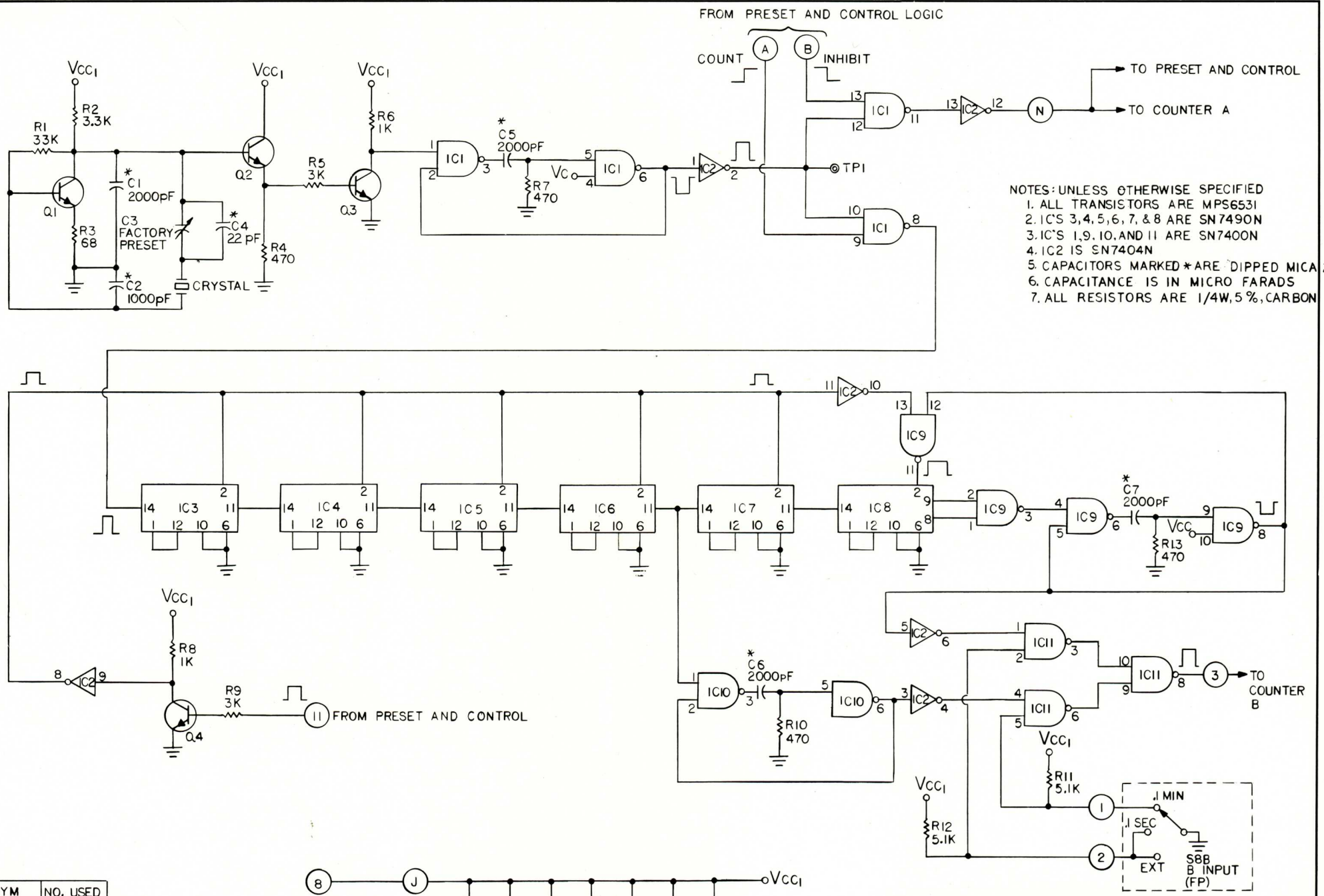


NOTES: UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTORS ARE $\frac{1}{4}$ W, 5%, CARBON
2. CAPACITORS MARKED (*) ARE DIPPED MICA
3. ALL RESISTORS MARKED (*) ARE $\frac{1}{8}$ W, 1% METAL FILM

Q3
IC9
C8
D1
R16

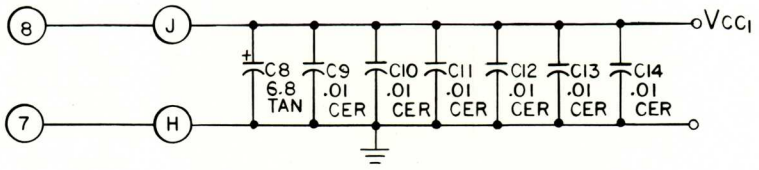
UNLESS OTHERWISE SPECIFIED DIMENSIONS IN INCHES TOLERANCES	ORTEC INCORPORATED		
FRACTIONS ±1/64 · DECIMALS XX ±.01 XXX ±.005 · ANGLES ±0°30' · FINISH 125	100 MIDLAND ROAD, OAK RIDGE, TENNESSEE 37830		
MATERIAL	TITLE: MODEL 715 DUAL COUNTER/TIMER TIME BASE		
APPLIED PRACTICES	DRAFTSMAN: J.D.W 10-23-69	RESPONSIBLE ENGINEER: E. OSTERTAG	REFERENCE
	CHECKED: BD	ENG. APPROVAL: R. Esterlund 2-21-70	STOCK NO.
	SCALE: +	MFG. APPROVAL: B Denning 3-12-70	DRAWING NO. 715-0801-SI
	DWG. ISSUED: Shirley 4-6-70	RELEASED FOR MFG.	

The transistor types installed in your instrument may differ from those shown in the schematic diagram. In such cases, necessary replacements can be made with either the type shown in the diagram or the type actually used in the instrument.



NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL TRANSISTORS ARE MPS6531
2. IC'S 3,4,5,6,7,& 8 ARE SN7490N
3. IC'S 1,9,10, AND 11 ARE SN7400N
4. IC2 IS SN7404N
5. CAPACITORS MARKED * ARE DIPPED MICA 2%.
6. CAPACITANCE IS IN MICRO FARADS
7. ALL RESISTORS ARE 1/4W, 5%, CARBON

SYM	NO. USED
R	1–13
C	1–14
Q	1–4
IC	1–11
S	8



UNLESS OTHERWISE SPECIFIED
DIMENSIONS IN INCHES
TOLERANCES
FRACTIONS ±1/64 | DECIMALS XX ±.01 XXX ±.005 | ANGLES ±0°30' | FINISH RMS
MATERIAL
APPLIED PRACTICES

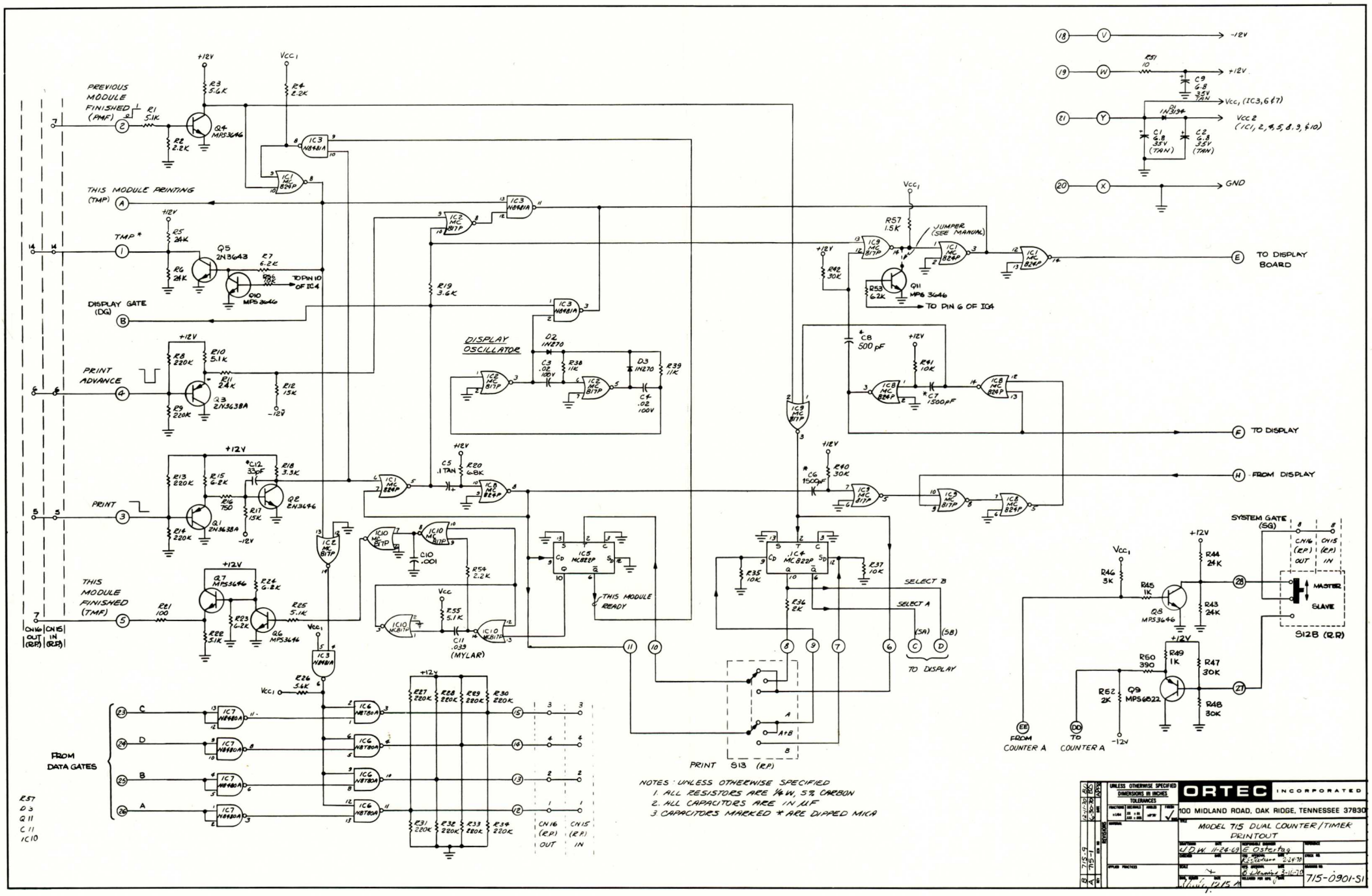
REVISIONS: BY | DATE | ECN NO | REV
BO | 2-11-71 | 715-10 | A

ORTEC INCORPORATED
100 MIDLAND ROAD, OAK RIDGE, TENNESSEE 37830

TITLE: MODEL 715 CRYSTAL TIME BASE

DRAFTSMAN: JDW	DATE: 10-3-70	RESPONSIBLE ENGINEER: R. Esteverena	REFERENCE
CHECKED	DATE	ENG. APPROVAL: [signature]	DATE 11-24-70	STOCK NO.
SCALE: ~		MFG APPROVAL: B. [signature]	DATE 11-23-70	DRAWING NO. 715-1601-S1
DWG. RELEASE: [signature]	DATE 12-10-70	RELEASED FOR MFG.	DATE

The transistor types installed in your instrument may differ from those shown in the schematic diagram. In such cases, necessary replacements can be made with either the type shown in the diagram or the type actually used in the instrument.


PREVIOUS MODULE FINISHED (PMF)
THIS MODULE PRINTING (TMP)
TMP *
DISPLAY GATE (DG)
PRINT ADVANCE
PRINT
THIS MODULE FINISHED (TMF)
FROM DATA GATES
DISPLAY OSCILLATOR
THIS MODULE READY
SELECT B
SELECT A
PRINT S13 (R.P.)
TO DISPLAY BOARD
TO DISPLAY
FROM DISPLAY
TO DISPLAY
FROM COUNTER A
TO COUNTER A
SYSTEM GATE (SG)
MASTER
SLAVE
S12B (R.P.)
-12V
GND
Vcc, (IC3, 6 & 7)
Vcc 2 (IC1, 2, 4, 5, 8, 9, & 10)
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 1/4 W, 5% CARBON
2. ALL CAPACITORS ARE IN µF
3. CAPACITORS MARKED * ARE DIPPED MICA
R57 D3 Q11 C11 IC10
ORTEC INCORPORATED
100 MIDLAND ROAD, OAK RIDGE, TENNESSEE 37830
MODEL 715 DUAL COUNTER/TIMER PRINTOUT
715-0901-S1

The transistor types installed in your instrument may differ from those shown in the schematic diagram. In such cases, necessary replacements can be made with either the type shown in the diagram or the type actually used in the instrument.

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE $\frac{1}{4}$ W, 5%, CARBON
2. ALL CAPACITORS ARE IN μF

(R.P.)
T1
Y24-132

REAR PANEL

VH247

MODULE POWER INPUT (R.P.)

34 GND
33 BLACK HOT
115 Vac
41 NEUT BLACK
16 +12V
17 -12V

GREEN
SC1
GREEN

D1

F1
3AG
2.5A
(FAST ACTING)

Q1
MJE 3055

H 7 → Vcc (4.8V) TO ALL BOARDS

9 10 K L

+12V
R1
33Ω
2W

TEST POINT

J

HEAT SINK

5 G E F

GND

C1
5000
10V

C2
5000
10V

C3
5000
10V

Q2
2N3053

R2
200Ω
(20T)

R3
300Ω

D3
IN4728

TO TIME BASE

SC2
RED
12

SC2
RED
11

D2

(−) (+)

+H.V. (225V)

N → TO DISPLAY BOARD

R4
240K
½W

C4
10
250V

GIW04

+12V
D 4

C5
6.8 (TAN)
35V

-12V
C 3

C6
6.8 (TAN)
35V

D3
C6
Q2
R4

REVISIONS	REV	ECN NO	DATE	APP
	A	715-7	10-3-70	BD

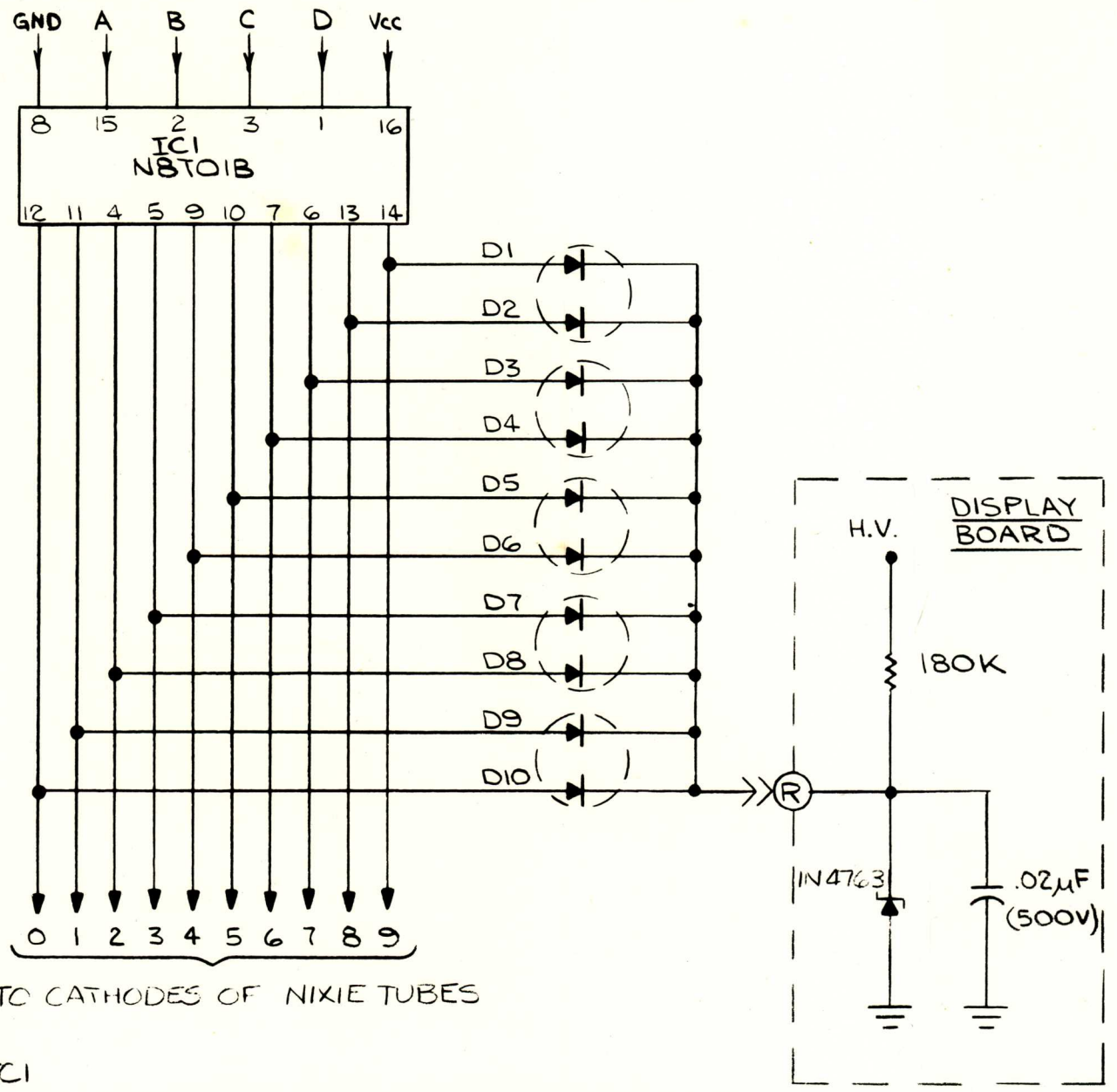
UNLESS OTHERWISE SPECIFIED
DIMENSIONS IN INCHES
TOLERANCES
FRACTIONS ±1/64 | DECIMALS XX ±.01 XXX ±.005 | ANGLES ±0°30' | FINISH ✓ RMS
MATERIAL
APPLIED PRACTICES

ORTEC INCORPORATED
100 MIDLAND ROAD, OAK RIDGE, TENNESSEE 37830

TITLE: 715 DUAL COUNTER/TIMER POWER SUPPLY

DRAFTSMAN DATE: D.NOE 11-19-69	RESPONSIBLE ENGINEER: E.OSTERTAG	REFERENCE	
CHECKED DATE	ENG. APPROVAL DATE: 3-2-70	STOCK NO.	
SCALE: NONE	MFG. APPROVAL DATE: B. Denning 3-12-70	DRAWING NO.	715-1001-S1
DWG. ISSUED DATE: Shirley 10-22-70	RELEASED FOR MFG. DATE		

The transistor types installed in your instrument may differ from those shown in the schematic diagram. In such cases, necessary replacements can be made with either the type shown in the diagram or the type actually used in the instrument.



IC1

D1 TO D10: 5 ea MSD 6100

UNLESS OTHERWISE SPECIFIED
DIMENSIONS IN INCHES
TOLERANCES

FRACTIONS	DECIMALS	ANGLES	FINISH
±1/64	XX ±.01 XXX ±.005	±0°30'	✓ RMS

MATERIAL

APPLIED PRACTICES

REVISIONS | ECN NO. | DATE | BY | REV

ORTEC INCORPORATED

100 MIDLAND ROAD, OAK RIDGE, TENNESSEE 37830

TITLE: 715 DUAL COUNTER/TIMER DECODER

DRAFTSMAN: DC — DATE: 11-3-69	RESPONSIBLE ENGINEER: E.OSTERTAG	REFERENCE	
CHECKED — DATE	ENG. APPROVAL: R Osterstag — DATE: 2-24-70	STOCK NO.	
SCALE	MFG. APPROVAL: B Deming — DATE: 4-28-70	DRAWING NO.	715-1101-S1
DWG. ISSUED: Shirley — DATE: 4-28-70	RELEASED FOR MFG. — DATE		

For more information on ORTEC products or their applications, contact your local ORTEC representative or:

Europe: ORTEC GmbH, 8 Munich 13, Frankfurter Ring 81, West Germany, Telephone (0811) 359-1001 or 359-1441, Telex 528476

United Kingdom: ORTEC Limited, Dallow Road, Luton, Bedfordshire, England, Telephone LUton 27557, Telex 82477

Other: ORTEC Incorporated, 100 Midland Road, Oak Ridge, Tennessee 37830, Telephone (615) 482-4411, TWX 810-572-1078, Telex 055-7450

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